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Implementation of Three phase SPWM Inverter with Minimum Number of Power Electronic Components

Muthyala Sarath[1] | V S N Narasimha Raju[2] | Seshagiri Boppana[3]

[1]Department of Electrical & Electronics Engineering, Vishnu Institute of Technology
[2]Assistant Professor,Department of Electrical & Electronics Engineering, Vishnu Institute of Technology
[3]Assistant Professor,Department of Electrical & Electronics Engineering, Vishnu Institute of Technology

ABSTRACT

In the past decades, the researchers have dealt with the conventional topology, which possesses sum switches of Multilevel Inverter is applied to PWM method. The present research work has been introduced a new method of multilevel inverter using reduced switches is applied with PWM technique. In introduction part the conventional new multilevel inverter & switching pattern are explained. In second part PWM technique of proposed work and circuits is explained. The width of this pulses are modulated in order to obtain inverter output voltage control and to reduce its harmonic content. Sinusoidal pulse width modulation or SPWM is the most common method in motor control and inverter application. Conventionally, to generate the signal, triangle wave as a carrier signal is compared with the sinusoidal wave, whose frequency is the desired frequency.

KEYWORDS: *Bidirectional switch, fundamental frequency staircase modulation, multilevel inverter.*

I. INTRODUCTION

Nowadays, multilevel inverters have received more attention for their ability on high power and medium voltage operation and for other advantages such as high power quality, low order harmonics, lower switching losses and better electromagnetic interferences.[1]These cascaded multilevel inverter generate a stepped voltage waveform, and more number of dc voltage waveform and switches will be used and they explain only the inverter operation and do not explain in different type of PWM technique is apply in proposed multilevel inverter.[2]These multilevel inverter is using a single phase seven level inverter for grid connected system. They are not explaining in different type of PWM technique is applied in proposed multilevel inverter.[3]These symmetric multilevel inverter introduce the least number of switches, and gate trigger circuitry, switching loss are reduced, cost and size, but it is implemented in basic sinusoidal pulse with modulation (SPWM) technique.[4] These cascaded multilevel inverter are using a nine and seven switches and sinusoidal pulse with modulation (SPWM) technique is also implemented using multicarrier wave signals, but they are not used in different type of PWM technique is apply in proposed multilevel inverter.[5-11]In recent years, different symmetric cascaded multilevel inverters have been presented, the main disadvantage of these circuits is some of them use a high number of bidirectional switches. More number of insulated gate bipolar transistors are required and they are not implemented in different type of PWM technique. a new topology of multilevel inverter is proposed in order to increase the number of output voltage levels and reduce the number of switches, drives circuit, total cost of the inverter, and implementation of different type of PWM technique. Moreover, the proposed topology is compared with other topologies from the different point of view. Such as number of IGBT, number dc sources and performances of different type of PWM technique. Finally, the performances of the proposed topology in generating are voltage levels through a seven levels inverter is confirmed by simulation using a (MATLAB/SIMULINK).

This paper presents how reduced harmonic distortion is achieved for a new topology of multilevel inverters using programmed without

PWM technique. This new topology has the advantage of its reduced number of switching devices compared to the conventional cascaded H-bridge and diode-clamped multilevel inverters for the same number of levels. It can also be extended to any number of levels. The modes of operation of a 5- level inverter are presented, where similar modes can be realized for higher levels. The inverter operation is controlled using switching angles based on without PWM with help of pulse generator.

II. Proposed Configuration

Fig. 1(a) and (b) shows the typical configuration of the proposed three-phase five-level multilevel inverter. Three bidirectional switches (S1–S6, Da1–Dc2), two switches–two diodes type, are added to the conventional three-phase two-level bridge (Q1–Q6). The function of these bidirectional switches is to block the higher voltage and ease current flow to and from the midpoint (o). A multilevel dc link built by a single dc voltage supply with fixed magnitude of $4V_{dc}$ and CHB having two unequal dc voltage supplies of V_{dc} and 2Vdc are connected to (+,–,o) bridge terminals. Based on the desired number of output voltage levels, a number of CHB cells are used. Since the proposed inverter is designed to achieve five voltage levels, the power circuit of the CHB makes use of two series cells having two unequal dc voltage supplies. In each cell, the two switches are turned ON and OFF under inverted conditions to output two different voltage levels. The first cell dc voltage supply V_{dc} is added if switch T1 is turned ON leading to V_{mg} $=+V_{dc}$ where V_{mg} is the voltage at node (m)with respect to inverter ground (g)or bypassed if switch T2 is turned ON leading to V_{mg} = 0. Likewise, the second cell dc voltage supply 2Vdc is added when switch T3 is turned ON resulting in V_{om} $=+2V_{dc}$ where V_{om} is the voltage at midpoint(o)with respect to node(m)or bypassed when switch T4 is turned ON resulting in V_{om} =0. The peak voltage rating of the switches of the conventional two level bridge (Q1–Q6) is 4Vdcwhereas the bidirectional switches (S1–S6) have a peak voltage rating of Vdc. In CHB cells, the peak voltage rating of second cell switches (T3 and T4) is $2V_{dc}$ while the peak voltage rating of T1 and T2 in the first cell is V_{dc}.

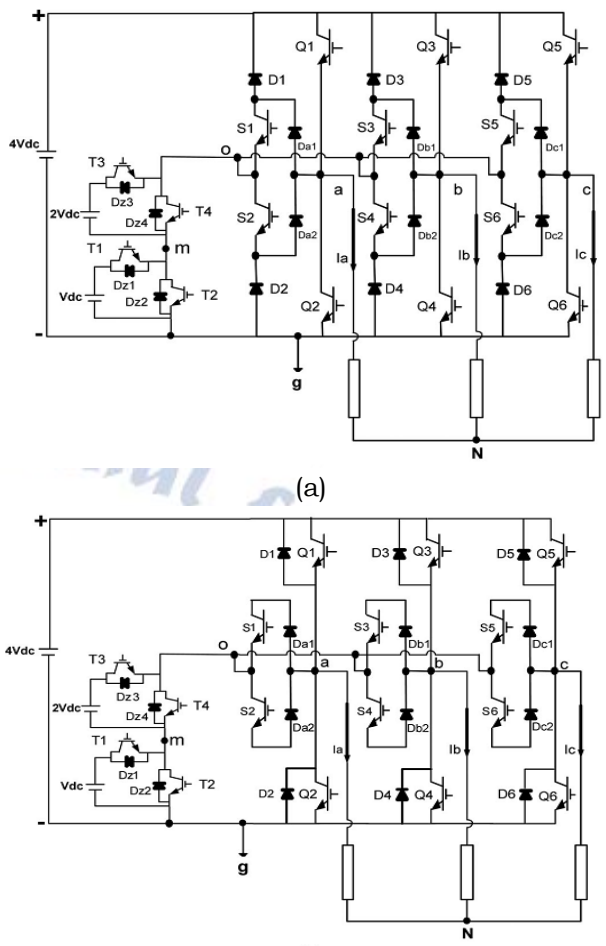

Fig. 1. Circuit diagram of the proposed three-phase five-level multilevel inverter.

TABLE I

Switching State S_a and Inverter Line-to-Ground Voltage V_{ag}

Sa	Q1	S1	S2	Q2	T1	T2	T3	T4	Vag
4	on	off	off	off	on	off	on	off	+4Vdc
3	off	on	on	off	on	off	on	off	+3Vdc
2	off	on	on	off	off	on	on	off	+2Vdc
1	off	on	on	off	on	off	off	on	+Vdc
0	off	off	off	on	on	off	off	on	0

It is easier to define the inverter line-to-ground voltages V_{ag}, V_{bg}, and V_{cg} in terms of switching states Sa, Sb, and Sc as

$$\begin{bmatrix} Vag \\ Vbg \\ Vcg \end{bmatrix} = \frac{4Vdc}{N-1} * \begin{bmatrix} Sa \\ Sb \\ Sc \end{bmatrix} \qquad (1)$$

Where N=5 is the maximum number of voltage levels.

The balanced load voltages can be achieved if the proposed inverter operates on the switching states depicted in Table II. The inverter may have 24 different modes within a cycle of the output waveform. According to Table II, it can be noticed

that the bidirectional switches operate in 18 modes. For each mode, there is no more than one bidirectional switch in on state. As a result, the load current commutates over one switch and one diode (for instance: in (410), the load current I_b can flow in S3 and Db1 or S4 and Db2). Since some insulated gate bipolar transistors (IGBTs) share the same switching gate signals, the proposed configuration significantly contributed in reducing the utilized gate driver circuits and system complexity. The inverter line-to-line voltage waveforms V_{ab},V_{bc}, and V_{ca} with corresponding switching gate signals are depicted in Fig. 2 where V_{ab}, V_{bc}, and V_{ca} are related to V_{ag}, V_{bg}, and V_{cg} by

$$\begin{bmatrix} Vab \\ Vbc \\ Vca \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} * \begin{bmatrix} Vag \\ Vbg \\ Vcg \end{bmatrix} \quad (2)$$

The inverter line-to-neutral voltages V_{aN}, V_{bN}, and V_{cN} may be expressed as

$$\begin{bmatrix} VaN \\ VbN \\ VcN \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} * \begin{bmatrix} Vag \\ Vbg \\ Vcg \end{bmatrix} \quad (3)$$

It is useful to recognize that the inverter voltages at terminals a, b, and c with respect to the midpoint (o) are given by

$$\begin{bmatrix} Vao \\ Vbo \\ Vco \end{bmatrix} = \begin{bmatrix} Vag \\ Vbg \\ Vcg \end{bmatrix} - \begin{bmatrix} Vog \\ Vog \\ Vog \end{bmatrix} \quad (4)$$

Where V_{og} is the voltage at midpoint(o)with respect to ground (g). V_{og} routinely fluctuates among three different voltage valuesVdc,2Vdc, and 3Vdcas follows:

$$\text{Vog} = \begin{cases} Vdc & if\ \ Sa + Sb + Sc \leq 5 \\ 2Vdc & if\ Sa + Sb + Sc = 6 \\ 3Vdc & if\ Sa + Sb + Sc \geq 7 \end{cases} \quad (5)$$

TABLE II
SWITCHINGSTATESSEQUENCE OF THE PROPOSEDINVERTERWITHINONECYCLE

Sa Sb Sc	Period T[s]	ON switches Leg a	ON switches Leg b	ON switches Leg c	ON switches Cascaded Half-bridge	Vag [V]	Vbg [V]	Vcg [V]
400	t1	Q1	Q4	Q6	T1,T4	4Vdc	0	0
410	t2	Q1	S3, S4	Q6	T1,T4	4Vdc	Vdc	0
420	t3	Q1	S3, S4	Q6	T2,T3	4Vdc	2Vdc	0
430	t4	Q1	S3, S4	Q6	T1,T3	4Vdc	3Vdc	0
440	t5	Q1	Q3	Q6	T1,T3	4Vdc	4Vdc	0
340	t6	S1, S2	Q3	Q6	T1,T3	3Vdc	4Vdc	0
240	t7	S1, S2	Q3	Q6	T2,T3	2Vdc	4Vdc	0
140	t8	S1, S2	Q3	Q6	T1,T4	Vdc	4Vdc	0
040	t9	Q2	Q3	Q6	T1,T4	0	4Vdc	0
041	t10	Q2	Q3	S5, S6	T1,T4	0	4Vdc	Vdc
042	t11	Q2	Q3	S5, S6	T2,T3	0	4Vdc	2Vdc
043	t12	Q2	Q3	S5, S6	T1,T3	0	4Vdc	3Vdc
044	t13	Q2	Q3	Q5	T1,T3	0	4Vdc	4Vdc
034	t14	Q2	S3, S4	Q5	T1,T3	0	3Vdc	4Vdc
024	t15	Q2	S3, S4	Q5	T2,T3	0	2Vdc	4Vdc
014	t16	Q2	S3, S4	Q5	T1,T4	0	Vdc	4Vdc
004	t17	Q2	Q4	Q5	T1,T4	0	0	4Vdc
104	t18	S1, S2	Q4	Q5	T1,T4	Vdc	0	4Vdc
204	t19	S1, S2	Q4	Q5	T2,T3	2Vdc	0	4Vdc
304	t20	S1, S2	Q4	Q5	T1,T3	3Vdc	0	4Vdc
404	t21	Q1	Q4	Q5	T1,T3	4Vdc	0	4Vdc
403	t22	Q1	Q4	S5, S6	T1,T3	4Vdc	0	3Vdc
402	t23	Q1	Q4	S5, S6	T2,T3	4Vdc	0	2Vdc
401	t24	Q1	Q4	S5, S6	T1,T4	4Vdc	0	Vdc

III. SWITCHING ALGORITHM

The staircase modulation can be simply implemented for the proposed inverter. Staircase modulation with selective harmonic is the most common modulation technique used to control the fundamental output voltage as well as to eliminate the undesirable harmonic components from the output waveforms. An iterative method such as the Newton–Raphson method is normally used to find the solutions to (N–1) nonlinear transcendental equations. The difficult calculations and the need of high performance controller for the real

application are the main disadvantages of such method. Therefore, an alternative method is proposed to generate the inverter's switching gate signals. It is easier to control the proposed inverter and achieve the required output voltage waveforms in terms of Sa, Sb, and Sc. The operation of the proposed inverter, the switching states Sa, Sb, and Scare determined instantaneously.

The on-time calculations of Sa, Sb, and Sc directly depend on the instantaneous values of the inverter line-to-ground voltages. It is well known that the reference values of Vag, Vbg, and Vcg are normally given by

$$\begin{bmatrix} Vag\_ref \\ Vbg\_ref \\ Vcg\_ref \end{bmatrix} = \frac{Ma*4Vdc}{2}\begin{bmatrix} \cos(wt) \\ \cos(wt-\frac{2\pi}{3}) \\ \cos(wt+\frac{2\pi}{3}) \end{bmatrix} + \frac{4Vdc}{2} * \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (6)$$

Where wt is the electrical angle Or

$$\begin{bmatrix} Vag_{ref} \\ Vbg_{ref} \\ Vcg_{ref} \end{bmatrix} = \frac{Ma*4Vdc}{2}\begin{bmatrix} \cos(wt) \\ \cos\left(wt-\frac{2\pi}{3}\right) \\ \cos\left(wt+\frac{2\pi}{3}\right) \end{bmatrix} + \frac{4Vdc}{2} * \left[1-\frac{Ma}{6}\cos(3wt)\right] * \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (7)$$

IV. Extended Structure

Level Shifted PWM Scheme (LSPWM)

Level shifted PWM (LS-PWM) is used for controlling voltage of a diode clamped multilevel inverter. The control principle of the level shifted SPWM is to use several triangular carrier signals keeping only one modulating sinusoidal signal. For a three level inverter two carriers and for a five level inverter, four triangular carriers are needed. In general if an m-level inverter is employed, (m-1) carriers are needed. The carriers have the same frequency f_c and the same peak-to-peak amplitude A_C. The zero reference is placed in the middle of the carrier set. The modulating signal is a sinusoid of frequency f_m and amplitude A_m. At every instant, each carrier is compared with the modulating signal. Each comparison switches the switch "on" if the modulating signal is greater than the triangular carrier assigned to that switch.

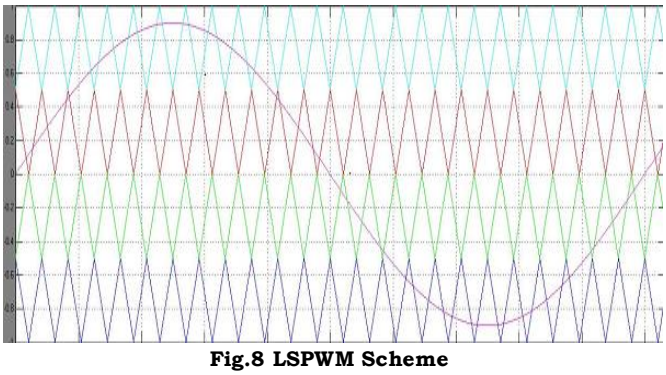

Fig.8 LSPWM Scheme

V. MATLAB/Simulink Results

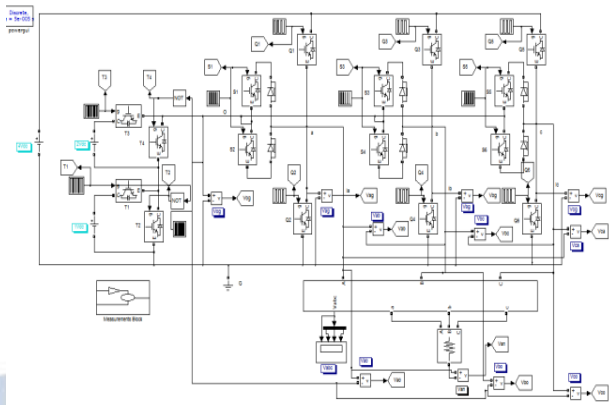

Fig .4. Simulink model of the proposed three-phase five-level multilevel inverter.

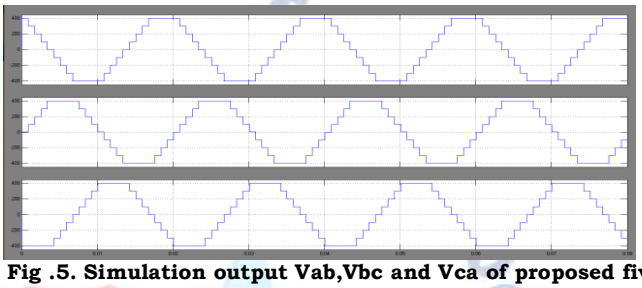

Fig .5. Simulation output Vab,Vbc and Vca of proposed five level inverter.

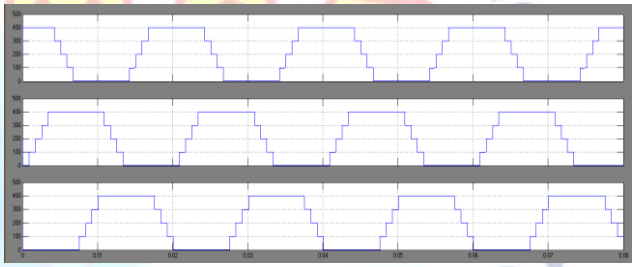

Fig .6. Simulation output Vag,Vbg and Vcg of proposed five level inverter.

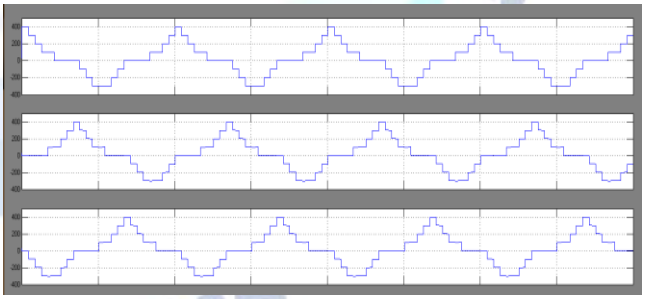

Fig .7. Simulation output Vao,Vbo and Vco of proposed five level inverter.

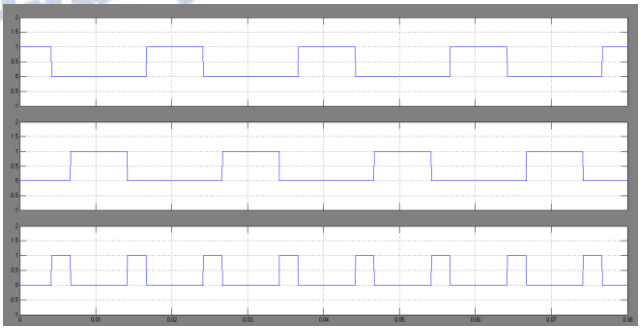

Fig .8. Simulated output wave forms of Q1, Q2 and S1.

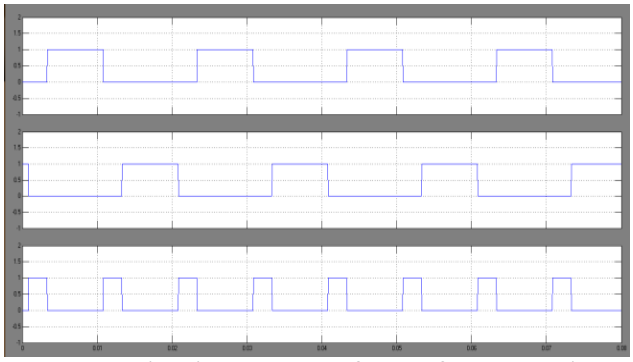

Fig .9. Simulated output wave forms of Q3, Q4 and S3.

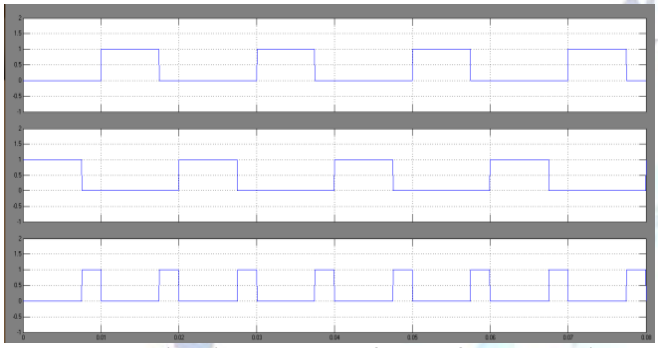

Fig .10. Simulated output wave forms of Q5, Q6 and S5.

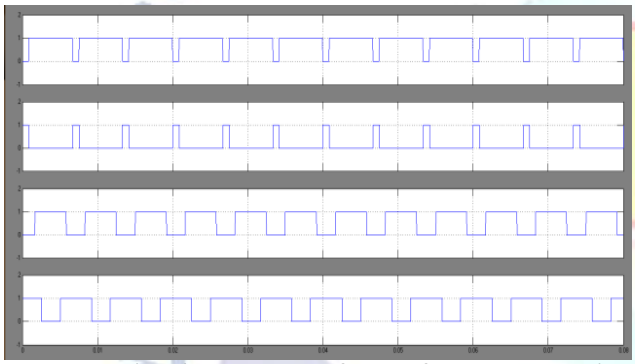

Fig .11. Simulated output wave forms of T1, T2, T3 and T4.

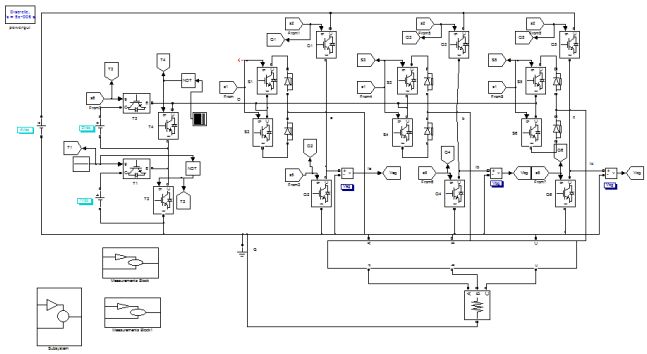

Fig .12.Simulink Model of the Proposed three-phase five-level multilevel inverter with PWM.

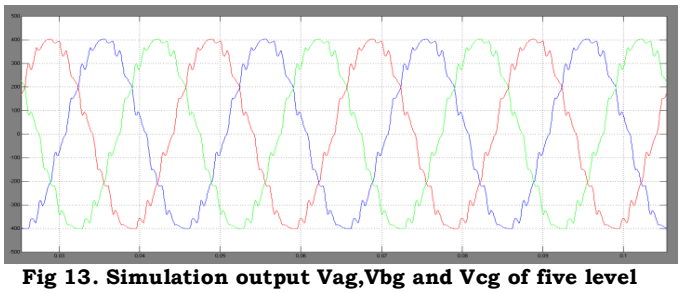

Fig 13. Simulation output Vag,Vbg and Vcg of five level inverter by using filter.

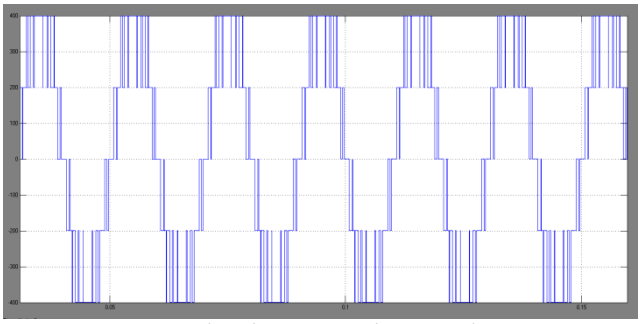

Fig.14.Five level output voltage with SPWM.

VI. Conclusion

A new topology of the three-phase seven-level multilevel inverter was introduced. The suggested configuration was obtained from reduced number of power electronic components. Therefore, the proposed topology results in reduction of installation area and cost. The different switching techniques and switching elements were used in single phase inverter also considered when inverters become the best power supply for converting DC power to AC power. Based on studied, SPWM techniques is a common method used in single phase inverter circuit are unipolar and Bipolar voltage Switching. The simulation of the single phase unipolar voltage switching inverter device model is simulated in Matlab/Simulink.

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