

Modeling of CHB Multilevel Inverter Based DSTATCOM for Reactive Power and Harmonics Compensation

Ch.Ashok Kumar¹ | S.Jayalakshmi² | S.Subramanya Sarma³

¹PG Scholar, Department of EEE, Ramachandra College of Engineering, Eluru, A.P, India.

²Professor & HOD, Department of EEE, Ramachandra College of Engineering, Eluru, A.P, India.

³ Associate Professor, Department of EEE, Ramachandra College of Engineering, Eluru, A.P, India.

To Cite this Article

Ch.Ashok Kumar, S.Jayalakshmi and S.Subramanya Sarma, "Modeling of CHB Multilevel Inverter Based DSTATCOM for Reactive Power and Harmonics Compensation", *International Journal for Modern Trends in Science and Technology*, Vol. 03, Issue 05, May 2017, pp. 165-169.

ABSTRACT

This paper presents an investigation of five-Level Cascaded H - bridge (CHB) Inverter as Distribution Static Compensator (DSTATCOM) in Power System (PS) for compensation of reactive power and harmonics. The advantages of CHB inverter are low harmonic distortion, reduced number of switches and suppression of switching losses. The DSTATCOM helps to improve the power factor and eliminate the Total Harmonics Distortion (THD) drawn from a Non-Linear Diode Rectifier Load (NLDRL). The D-Q reference frame theory is used to generate the reference compensating currents for DSTATCOM while Proportional and Integral (PI) control is used for capacitor DC voltage regulation. A CHB Inverter is considered for shunt compensation of a 11 kV distribution system. Finally a level shifted PWM (LSPWM) and phase shifted PWM (PSPWM) techniques are adopted to investigate the performance of CHB Inverter. The results are obtained through MATLAB/SIMULINK software package.

KEYWORDS — DSTATCOM, Harmonic compensation, Level shifted PWM, Phase shifted PWM, CHB multilevel inverter D-Q reference frame

*Copyright © 2017 International Journal for Modern Trends in Science and Technology
All rights reserved.*

I. INTRODUCTION

Modern power systems are of complex networks, where hundreds of generating stations and thousands of load centers are interconnected through long power transmission and distribution networks. Even though the power generation is fairly reliable, the quality of power is not always so reliable. Power distribution system should provide with an uninterrupted flow of energy at smooth sinusoidal voltage at the contracted magnitude level and frequency to their customers. PS especially distribution systems, have numerous non linear loads, which significantly affect the quality of power. Apart from non linear loads, events like capacitor switching, motor starting and

unusual faults could also inflict power quality (PQ) problems. PQ problem is defined as any manifested problem in voltage/current or leading to frequency deviations that result in failure or maloperation of customer equipment. Voltage sags and swells are among the many PQ problems the industrial processes have to face. Voltage sags are more severe. During the past few decades, power industries have proved that the adverse impacts on the PQ can be mitigated or avoided by conventional means, and that techniques using fast controlled force commutated power electronics (PE) are even more effective. PQ compensators can be categorized into two main types. One is shunt connected compensation device that effectively

eliminates harmonics.

The other is the series connected device, which has an edge over the shunt type for correcting the distorted system side voltages and voltage sags caused by power transmission system faults. The STATCOM used in distribution systems is called DSTACOM (Distribution-STACOM) and its configuration is the same, but with small modifications. It can exchange both active and reactive power with the distribution system by varying the amplitude and phase angle of the converter voltage with respect to the line terminal voltage.

A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of output voltage levels. There are several types of multilevel inverters: cascaded R-bridge (CRB), neutral point clamped, flying capacitor [2-5]. In particular, among these topologies, CHB inverters are being widely used because of their modularity and simplicity. Various modulation methods can be applied to CHB inverters. CHB inverters can also increase the number of output voltage levels easily by increasing the number of R-bridges. This paper presents a DSTATCOM with a proportional integral controller based CHB multilevel inverter for the harmonics and reactive power mitigation of the nonlinear loads. This type of arrangements have been widely used for PQ applications due to increase in the number of voltage levels, low switching losses, low electromagnetic compatibility for hybrid filters and higher order harmonic elimination.

II. DESIGN OF MULTILEVEL BASED DSTATCOM

A. Principle of DSTATCOM

A D-STATCOM (Distribution Static Compensator), which is schematically depicted in Figure- I, consists of a two-level Voltage Source Converter (VSC), a dc energy storage device, a coupling transformer connected in shunt to the distribution network through a coupling transformer. The VSC converts the dc voltage across the storage device into a set of three-phase ac output voltages. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. Suitable adjustment of the phase and magnitude of the D-STATCOM output voltages allows effective control of active and reactive power exchanges between the DSTATCOM and the ac system. Such configuration

allows the device to absorb or generate controllable active and reactive power.

The VSC connected in shunt with the ac system provides a multifunctional topology which can be used for up to three quite distinct purposes:

1. Voltage regulation and compensation of reactive power;
2. Correction of power factor
3. Elimination of current harmonics.

Here, such device is employed to provide continuous voltage regulation using an indirectly controlled converter. As shown in Figure-1 the shunt injected current I_{sh} corrects the voltage sag by adjusting the voltage drop across the system impedance Z_{th} . The value of I_{sh} can be controlled by adjusting the output voltage of the converter. The shunt injected current I_{sh} can be written as,

$$I_{sh} = I_L - I_S = I_L - \frac{(V_L - V_S)}{Z_{th}} \quad (1)$$

The complex power injection of the D-STATCOM can be expressed as,

$$S_{sh} = V_L I_{sh} \quad (2)$$

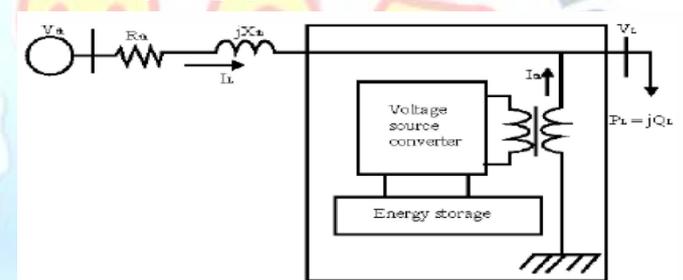


Figure 1 Schematic Diagram of a DSTATCOM

It may be mentioned that the effectiveness of the DSTATCOM in correcting voltage sag depends on the value of Z_{th} or fault level of the load bus. When the shunt injected current I_{sh} is kept in quadrature with V_L , the desired voltage correction can be achieved without injecting any active power into the system. On the other hand, when the value of I_{sh} is minimized, the same voltage correction can be achieved with minimum apparent power injection into the system.

B. Control for Reactive Power Compensation

The aim of the control scheme is to maintain constant voltage magnitude at the point where a sensitive load under system disturbances is connected. The control system only measures the rms voltage at the load point, i.e., no reactive power measurements are required. The VSC switching strategy is based on a sinusoidal PWM technique which offers simplicity and good response. Since custom power is a relatively low-power application,

PWM methods offer a more flexible option than the fundamental frequency switching methods favored in FACTS applications. Apart from this, high switching frequencies can be used to improve on the efficiency of the converter, without incurring significant switching losses.

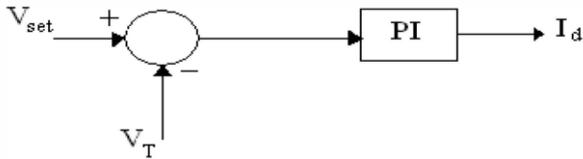


Figure 2 PI control for reactive power compensation

The controller input is an error signal obtained from the reference voltage and the rms terminal voltage measured. Such error is processed by a PI controller; the output is the angle θ , which is provided to the PWM signal generator. It is important to note that in this case, of indirectly controlled converter, there is active and reactive power exchange with the network simultaneously. The PI controller processes the error signal and generates the required angle to drive the error to zero, i.e. the load rms voltage is brought back to the reference voltage.

C. Control for Harmonics Compensation

The Modified Synchronous Frame method is presented in [7]. It is called the instantaneous current component (i_d-i_q) method. This is similar to the Synchronous Reference Frame theory (SRF) method. The transformation angle is now obtained with the voltages of the ac network. The major difference is that, due to voltage harmonics and imbalance, the speed of the reference frame is no longer constant. It varies instantaneously depending of the waveform of the 3-phase voltage system. In this method the compensating currents are obtained from the instantaneous active and reactive current components of the nonlinear load. However, the load current components are derived from a SRF based on the Park transformation.

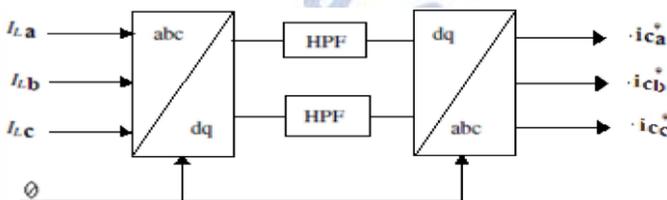


Figure 3 Block diagram of SRF method

Figure 3 shows the block diagram SRF method. Under balanced and sinusoidal voltage conditions angle θ is a uniformly increasing function of time. This transformation angle is sensitive to voltage harmonics and unbalance.

D. Cascaded H-Bridge Multilevel Inverter

Figure 4 shows the circuit model of a single CHB inverter configuration. By using single H-Bridge we can get voltage levels. The number of output voltage levels of CHB is given by $2n+1$ and voltage step of each level is given by $V_{dc}/2n$, where n is number of R-bridges connected in cascaded. The switching table is given in Table 1.

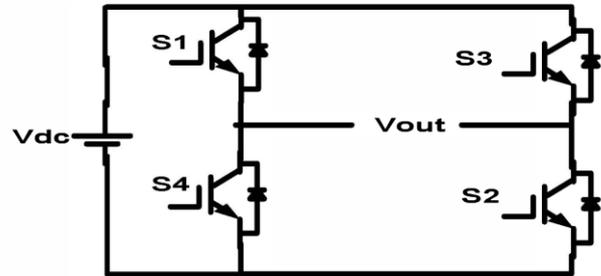


Figure 4 Circuit of the single cascaded H-Bridge Inverter

Table-1 Switching table of single CHB inverter

Switches Turn ON	Voltage Level
S1,S2	V _{dc}
S3,S4	-V _{dc}
S4,D2	0

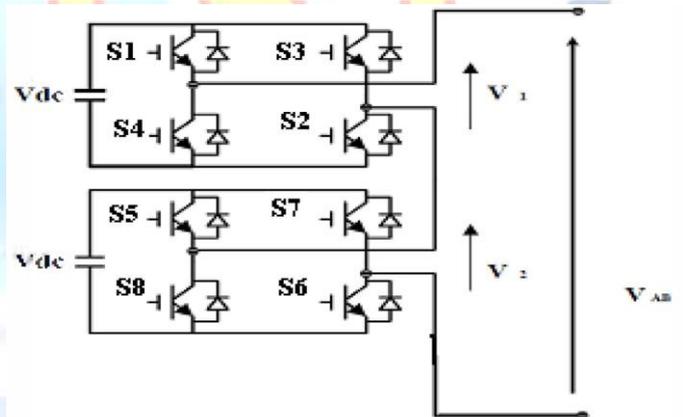


Figure 5 Block diagram of 5-level CHB inverter model

The switching mechanism for 5-level CHB inverter is shown in table-2.

Table 2 Switching table for 5-level CHB Inverter

Switches Turn On	Voltage Level
S1, S2	V _{dc}
S1,S2,S5,S6	2V _{dc}
S4,D2,S8,D6	0
S3,S4	-V _{dc}
S3,S4,S7,S8	-2V _{dc}

E. Design of Single H-Bridge Cell

Steps to design the single H-bridge cell

- Device Current
- IGBT Loss Calculation

- Diode Loss Calculation
- Thermal Calculations

F. DC-Capacitor Selection

The required capacitance for each cell depends on the allowable ripple voltage and the load current. The rms ripple current flowing into the capacitor can be written as follows and the ripple current frequency is double the load current frequency.

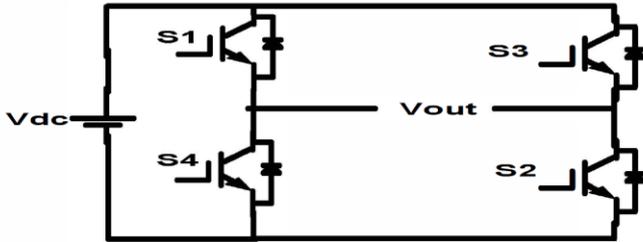


Figure 6 H-Bridge converter

G. PWM Techniques for CHB Inverter

The most popular PWM techniques for CHB inverter are

1. Phase Shifted Carrier PWM (PSCPWM)
2. Level Shifted Carrier PWM (LSCPWM).

1. Phase Shifted Carrier PWM (PSCPWM)

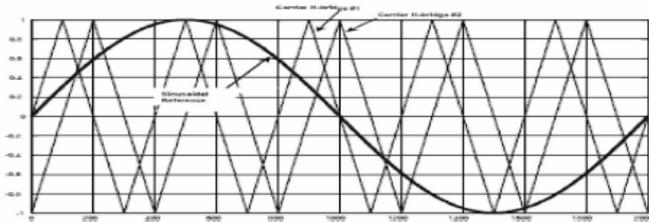


Figure 7 Phase shifted carrier PWM

Figure 7 shows the Phase shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal uni polar pulse width modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells. A carrier phase shift of $180^\circ/m$ (No. of levels) for cascaded inverter is introduced across the cells to generate the stepped multi level output waveform with lower distortion.

2. Level Shifted Carrier PWM (LSCPWM)

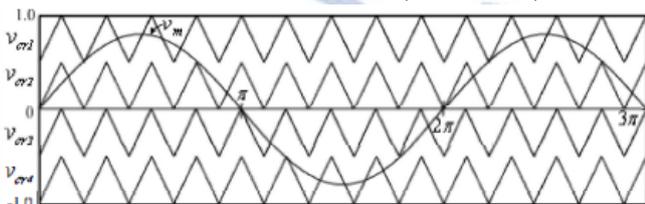


Figure 8 Level shifted carrier PWM

Figure 8 shows the Level shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal unipolar width modulation and bipolar pulse width modulation

respectively, providing an even power distribution among the cells. A carrier Level shift by 1m (No. of levels) for cascaded inverter is introduced across the cells to generate the stepped multilevel output waveform with lower distortion.

III. MATLAB/SIMULINK MODELING AND SIMULATION RESULTS

Figure 9 shows the MATAB/SIMULINK power circuit model of DSTATCOM. It consists of five blocks named as source block, non linear load block, control block, APF block and measurements block. The system parameters for simulation study are source voltage of 11kV, 50 Hz AC supply, DC bus capacitance 1500e-6 F, Inverter series inductance 10 mH, Source resistance of 0.1 ohm and inductance of 0.9 mH, Load resistance and inductance are chosen as 30mH and 60 ohms respectively.

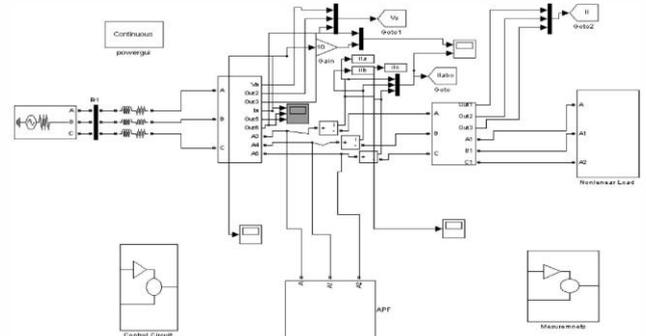


Figure 9 MATLAB/SIMULINK power circuit model of DSTATCOM

Figure 10 shows the phase- A voltage of five level output of phase shifted carrier PWM inverter.

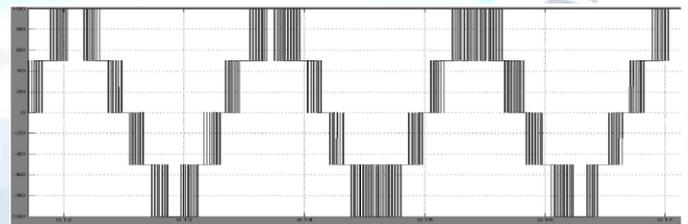


Figure 10 five level PSCPWM output

Figure 11 shows the three phase source voltages, three phase source currents and load currents respectively without DSTATCOM. It is clear that without DSTATCOM load current and source currents are same.

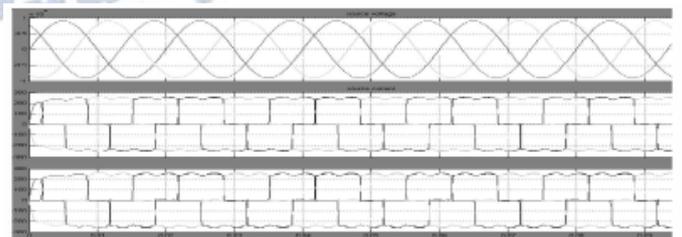


Figure 11 Source voltage, current and load current without DSTATCOM

Figure-12 shows the three phase source voltages, three phase source currents and load currents respectively with DSTATCOM. It is clear that with DSTATCOM even though load current is non sinusoidal source currents are sinusoidal.

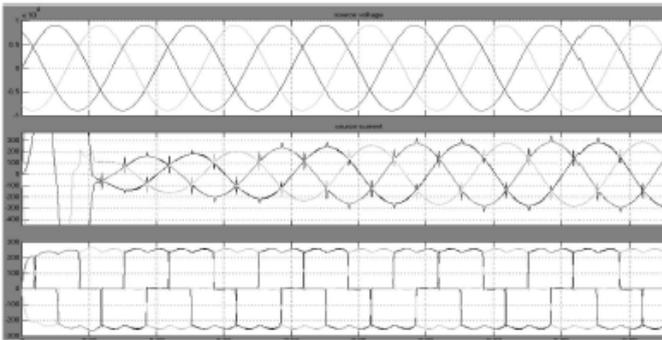


Figure-12 Source voltage, current and load current with DSTATCOM

Figure 13 shows the DC bus voltage. The DC bus voltage is regulated to 11kV by using PI regulator.

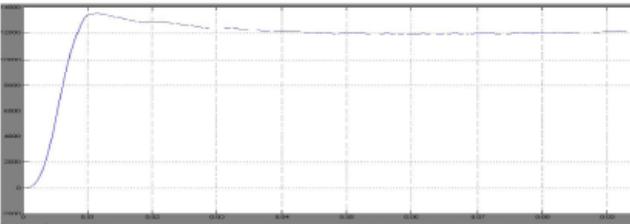


Figure 13 DC Bus Voltage

Figure 14 shows the phase- A source voltage and current, even though the load is non linear RL load the source power factor is unity.

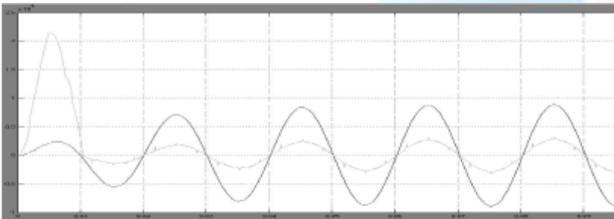


Figure 14 Phase-A source voltage and current

Figure 15 shows the harmonic spectrum of Phase - A Source current without DSTATCOM. The THD of source current without DSTATCOM is 36.89%.

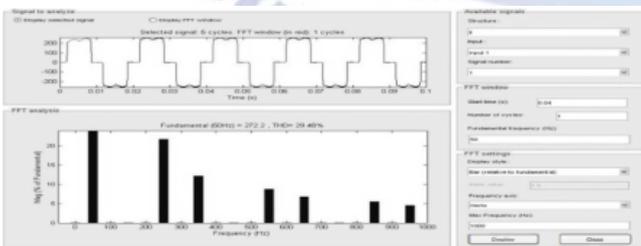


Figure 15 Harmonic spectrum of Phase-A Source current without DSTATCOM

Figure 16 shows the harmonic spectrum of Phase A Source current with DST ATCOM. The THD of source current without DST ACOM is 5.05%

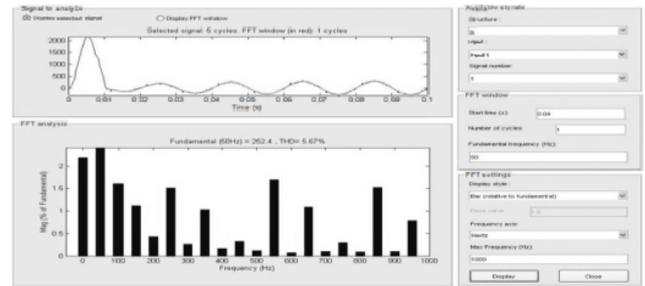


Figure 16 Harmonic spectrum of Phase-A Source current with DSTATCOM

IV. CONCLUSIONS

A DSTATCOM with five level CHB inverter is investigated. Mathematical model for single H-Bridge inverter is developed which can be extended to multi H-Bridge. The source voltage, load voltage, source current, load current, power factor simulation results under nonlinear loads are presented. Finally MATLAB/SIMULINK based model is developed and simulation results are presented.

REFERENCES

- [1] K.A Corzine. and Y.L Familiant, "A New Cascaded Multi-level H Bridge Drive:' IEEE Trans. Power.Electron .• vol. I 7. no. I. pp. I 25-I 3 I. Jan 2002.
- [2] J.S.Lai. and F.Z.Peng "Multilevel converters - A new bread of converters, "IEEE Trans. Ind.Appli .• vol.1.32. no.3. pp.S09-S17. May/ Jun. 1996.
- [3] T.A.Maynard. M.Fadel and N.Aouda. "Modelling of multilevel converter:' IEEE Trans. Ind.Electron .• vol.1.44. pp.3S6-364. Jun. I 997.
- [4] P.Bhagwat. and V.R.Stefanovic. "Generalized structure of a multilevel PWM Inverter:' IEEE Trans. Ind. Appln, Vol.IA-19. no.6, pp. I OS7-1069, Nov.!Dec .. 1983.
- [5] J.Rodriguez. Jih-sheng Lai, and F Zheng peng, "Multilevel Inverters; A Survey of Topologies, Controls, and Applications," IEEE Trans. Ind. Electron., vol.49 , n04., pp.724-738. Aug. 2002.
- [6] Roozbeh Naderi, and Abdolreza rahmati, "Phase-shifted carrier PWM technique for general cascaded inverters," IEEE Trans. Power.Electron., vol.1.23, no.3, pp. I 257-I 269. May. 2008.
- [7] Bhim Singh, Kamal AlHaddad & Ambrish Chandra, 1999, A Review of Active Filter for Power Quality Improvements, IEEE Trans on Industrial Electronics, 46(S), pp.960970
- [8] Mauricio Angulo, Pablo Lezana, Samir Kouro, Jos'e Rodrl'guez and Bin Wu, "Level-shifted PWM for Cascaded Multilevel Inverters with Even Power Distribution" IEEE Power Electronics specialist conference, 17-21 june 2007, pp.2373-2378.
- [9] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 858- 867, August 2002.