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Space-Grade VLSI Implementation: Error Detection and Correction Codes in Advanced Aerospace Systems

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ABSTRACT

This paper addresses the critical issue of bit errors in on-chip memories within a die due to various environmental factors such as cosmic radiation, alpha and neutron particles, and extreme temperatures in space, which can lead to data corruption as technology scales. To mitigate these errors, the paper introduces an innovative error correction technique based on a 2-dimensional code utilizing a divide-symbol approach, specifically designed to counteract radiation-induced Multiple Cell Upsets (MCUs) in memory for space applications. The encoding process involves analyzing data bits, diagonal bits, parity bits, and check bits through XOR operations. Data recovery is achieved by performing XOR operations between the encoded bits and the recalculated encoded bits. Subsequently, a comprehensive process encompassing analysis, verification, selection, and correction is executed. The proposed scheme is implemented and validated through simulation and synthesis using Xilinx ISE with Verilog HDL. Comparative analysis demonstrates that this encoding-decoding process not only achieves effective error correction but also minimizes power consumption, occupies minimal area, and incurs minimal delay compared to established methods.

Keywords: Error Correction Code (ECC), On-chip Memories, Radiation-induced Multiple Cell Upsets (MCUs), 2-dimensional Code, XOR Operation

1. INTRODUCTION

In computing, telecommunication, information theory, and coding theory, an error correction code, sometimes error correcting code, (ECC) is used for controlling errors in data over unreliable or noisy communication channels. The central idea is the sender encodes the message with redundant information in the form of an ECC. The redundancy allows the receiver to detect a limited number of errors that may occur anywhere in the message, and often to correct these errors without retransmission. The American mathematician Richard Hamming pioneered this field in the 1940s and invented the first error-correcting code in 1950: the Hamming (7,4) code.

ECC contrasts with error detection in that errors that are encountered can be corrected, not simply detected. The advantage is that a system using ECC does not require a reverse channel to request retransmission of data when an error occurs. The downside is that there is a fixed overhead that is added to the message, thereby

requiring a higher forward channel bandwidth. ECC is therefore applied in situations where retransmissions are costly or impossible, such as one-way communication links and when transmitting to multiple receivers in multicast. Long-latency connections also benefit; in the case of a satellite orbiting around Uranus, retransmission due to errors can create a delay of five hours. ECC information is usually added to mass storage devices to enable recovery of corrupted data, is widely used in modems, and is used on systems where the primary memory is ECC memory.

ECC processing in a receiver may be applied to a digital bit stream or in the demodulation of a digitally modulated carrier. For the latter, ECC is an integral part of the initial analog-to-digital conversion in the receiver. The Viterbi decoder implements a soft-decision algorithm to demodulate digital data from an analog signal corrupted by noise. Many ECC encoders/decoders can also generate a bit-error rate (BER) signal which can be used as feedback to fine-tune the analog receiving electronics.

The maximum fractions of errors or of missing bits that can be corrected is determined by the design of the ECC code, so different error correcting codes are suitable for different conditions. In general, a stronger code induces more redundancy that needs to be transmitted using the available bandwidth, which reduces the effective bit-rate while improving the received effective signal-to-noise ratio. The noisy-channel coding theorem of Claude Shannon answers the question of how much bandwidth is left for data communication while using the most efficient code that turns the decoding error probability to zero. This establishes bounds on the theoretical maximum information transfer rate of a channel with some given base noise level. However, the proof is not constructive, and hence gives no insight of how to build a capacity achieving code. After years of research, some advanced ECC systems nowadays come very close to the theoretical maximum.

The two main categories of ECC codes are block codes and convolutional codes.

Block codes work on fixed-size blocks (packets) of bits or symbols of predetermined size. Practical block codes can generally be hard-decoded in polynomial time to their block length.

Convolutional codes work on bit or symbol streams of arbitrary length. They are most often soft decoded with the Viterbi algorithm, though other algorithms are sometimes used. Viterbi decoding allows asymptotically optimal decoding efficiency with increasing constraint length of the convolutional code, but at the expense of exponentially increasing complexity. A convolutional code that is terminated is also a 'block code' in that it encodes a block of input data, but the block size of a convolutional code is generally arbitrary, while block codes have a fixed size dictated by their algebraic characteristics. Types of termination for convolutional codes include "tail-biting" and "bit-flushing".

There are many types of block codes, but among the classical ones the most notable is Reed-Solomon coding because of its widespread use in compact discs, DVDs, and hard disk drives. Other examples of classical block codes include Golay, BCH, Multidimensional parity, and Hamming codes.

Hamming ECC is commonly used to correct NAND flash memory errors. This provides single-bit error correction and 2-bit error detection. Hamming codes are only suitable for more reliable single-level cell(SLC) NAND. Denser multi-level cell (MLC) NAND requires stronger multi-bit correcting ECC such as BCH or Reed–Solomon.NOR Flash typically does not use any error correction.

Classical block codes are usually decoded using hard-decision algorithms, which means that for every input and output signal a hard decision is made whether it corresponds to a one or a zero bit. In contrast, convolutional codes are typically decoded using soft-decision algorithms like the Viterbi, MAP or BCJR algorithms, which process (discretized) analog signals, and which allow for much higher error-correction performance than hard-decision decoding.

Nearly all classical block codes apply the algebraic properties of finite fields. Hence classical block codes are often referred to as algebraic codes.

In contrast to classical block codes that often specify an error-detecting or error-correcting ability, many modern block codes such as LDPC codes lack such guarantees. Instead, modern codes are evaluated in terms of their bit error rates.

Most forward error correction codes correct only bit-flips, but not bit-insertions or bit-deletions. In this setting, the Hamming distance is the appropriate way to measure the bit error rate. A few forward error correction codes are designed to correct bit-insertions

and bit-deletions, such as Marker Codes and Watermark Codes. The Levenshtein distance is a more appropriate way to measure the bit error rate when using such codes.

2. LITERATURE REVIEW

In space, due to high temperatures, electronic circuits, in particular memories subject to soft errors lead to poor reliability. Memory cells are interrupted by neutron or alpha particles from earth's atmosphere [1]-[3]. One way to reduce these errors by maximizing the critical charge at the state nodes or by well and substrate techniques (process related techniques). Another way is, by applying error correction codes (ECC) on memories with that some errors can be overcome [4]. This is usually performed by single error correction (SEC) code on each memory to deal with independent errors. Scrubbing with SEC increases accuracy. It reads memory and corrects the single errors time to time; will not accumulate over time [5]. This is not effective for multiple cell upsets (MCUs) because in this MCU two or more bits of same memory gets affected. To overcome the multiple cell upsets in memories, interleaving method is proposed [6]. Many studies have been takes place with this technique to manage multiple cell upsets (MCUs). But this proposed interleaving method increases the system design complexity and shows impact in area and power consumption. So that ECCs is used in case for multiple cell upsets (MCUs). This requires more parity bits, more time for decoding the bits and more complex circuits are needed to perform for the encoding and decoding operations. Various ECCs focused to reduce area, delay and power.

Zhu et al., [7] proposes a new error correction code for the reduction of radiation exposed multiple bit upsets in memories. This detects and corrects the adjacent double bit errors and also lowers the errors for the non-adjacent double bit errors. The experimental results demonstrate that it reduces 40% hardware redundancy and more efficient compared to other existing ECC codes. Also, this method minimizes the errors for non-adjacent DBE by 12% when compared with the conventional SEC-DED-DAEC codes leads to high reliability memory system design. Pedro et al., [8] has introduced an efficient single and double adjacent error correcting parallel decoder for the (24, 12) extended Golay code. In this parallel decoder, first a 12 bit OR gate is used for the implementation of foremost and the rest is implemented using 24 bit OR gate. Using HDL, and with the mapping of TSMC 65 nm technology of synopsis design compiler synthesized twice to reduce the area and delay. That means, the reductions are around 45% and 11% for area and the reductions 28% and 21% for delay when relate with existing SEC- DAEC decoder. A new decimal matrix code ECC is used to enhance the memory reliability in [9]. The encoder and decoder are synthesized in SMIC 0.18 μm technology by synopsis design compiler. Simulation result shows that the MTTF of this technique is 452.9%, 154.6%, 122.6% and the delay is 73.1%, 69.0%, 26.2% for hamming, MC and PDS respectively.

Using different set of codes (cyclic-linear block codes) as ECC, protect the memory from data loss is proposed in [12]. This scheme exploits the localization of MCU errors, also the features of DS codes to enhance error correction possibilities and to reduce the decoding time. This is implemented in HDL and the simulation result indicates that this technique is effective in reducing the decoding time and also the area and power consumption. Reviregoet al., [13] suggested a new code to correct triple adjacent errors (SEC-DAEC-TAEC) and 3-bit burst errors for different data word lengths (16, 32 and 64 data bits). Two optimization criteria have been used; reducing the total number of ones in the parity check matrix minimizes decoding time and the maximum number of ones in its rows optimizes the speed. Andrew et al., [14] proposed a turbo system and also lowdensity parity-check code for space engineering. This turbo system and LPDC codes are widely used in the data transmission for the aircraft applications. The error correcting code with low power consumption from space has been introduced in an encoding-decoding manner. Low-density parity-check codes are organized in the form of parity check matrix, where the code rate reduces then this parity check matrix gets increases and therefore, this decoder is more complex. The development of the turbo codes and LPDC codes increases the efficiency and reliability of the system compared to the existing error correction codes in the deep space applications. Alternatively, turbo codes are formed on trellises. There will be one trellis section/information bit, for various code symbols.

Therefore, turbo codes are more superior to low-density parity-check codes at low rate. In comparison, with other decoding methods, this iterative decoding of either turbo or LDPC code is more complex. A new forward error correction code (FEC Encoder) is introduced for DVB S2 system with BCH code and LPDC code and also using QPSK modulation [15]. For FPGA implementation, the code length of 64800 bits and ½ codes normal rate LDPC code is considered. The design is processed at 122 MHz for timing specifications. Pipelining technology is also included in the design to improve the coding efficiency. In this paper, a new encoding-decoding algorithm is proposed for the error correction and detection in multiple cell upset (MCUs). For encoding, data bits, diagonal bits, parity bits and check bits were examined using the XOR operation. And to recover the original data, again XOR operation was performed between the redundancy bits and the recalculated redundancy bits. After analyzing, verification, selection and correction process takes place in the decoding process.

3.IMPLEMENTATION OF PROPOSED ARCHITECTURE

We propose using two-dimensional error correction code techniques on SRAM for the fast, error-free operation of common errors. The key to 2D error coding is the combination of lightweight horizontal per-word error coding and vertical column error coding. The horizontal and vertical coding can be an error detection code (EDC) or an error correction code (ECC). So we only use vertical codes for correcting errors, and keep them in the background, so they have a minimal overhead impact in the absence of errors.In order to demonstrate how 2D error code works, 2D error coding and Hamming code are compared and described below. The first is to compare two protection methods' error covering and memory requirements for 8 × 8 memory arrays. To enhance memory reliability, a new error correction 2-dimensional code (2D-ECC) is proposed. This algorithm detects and corrects errors effectively when relates with other existing error correction techniques. This performs data region division, redundancy and syndrome calculation, verification and region selection one by one to recover the original data. Boolean XOR operation is performed which is most widely used in cryptography and also in generating parity bits for error checking and fault tolerance. The block diagram of the proposed ECC methodology is shown in figure 1.

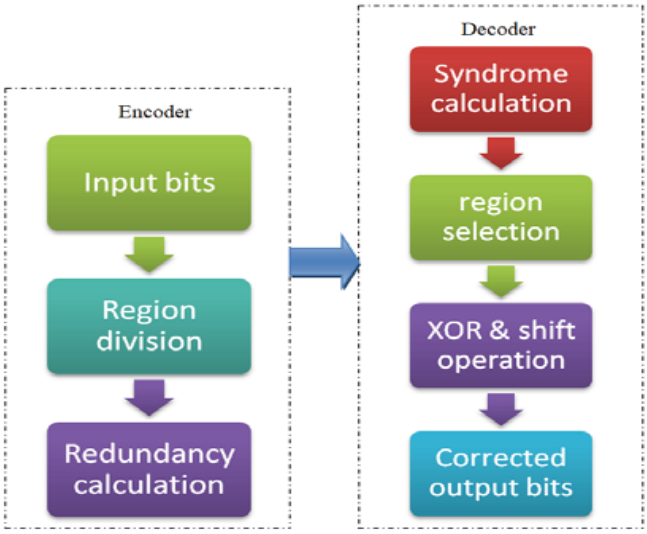

Figure 1: ECC methodology

This2-dimensional algorithm performs encoding-decoding process which codifies 16 bit input data into 32 bits in encoding and while decoding again the original 16 bit data is recovered.

3.1Proposed Algorithm

STEP 1: Read the input 16-bit data (A16 – A0)

STEP 2: Divide the input data into 4 groups

X_1	Y_1	Z_1	W_1
X_2	Y_2	Z_2	W_2
X_3	Y_3	Z_3	W_3
X_4	Y_4	Z_4	W_4

3.2Process of encoding

First, divide the 16 input bits into four groups (Xi, Yi, Zi, Wi). The diagonal bits (Di), parity bits (Pi) and check bits (Ci) are determined using XOR operation. In the process of encoding, the input 16 bits gets converted into 32 bits (redundancy bits).

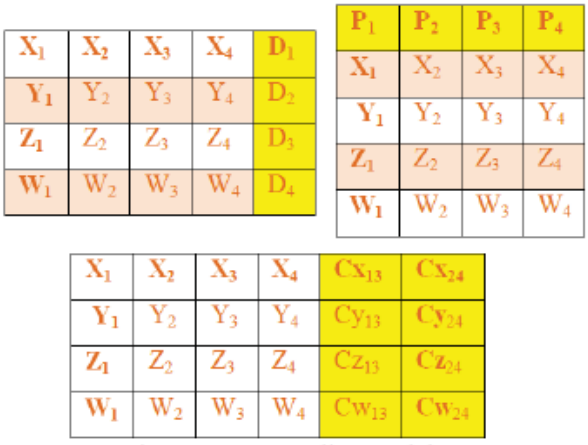

Figure 2: Encoding model

STEP 3: Analyze diagonal bits, parity bits and check bits using XOR operation.

i) Diagonal bits (D1, D2, D3, D4) using XOR operation as the 2×2 matrix,

$$D_1 = X_1 \oplus Y_2 \oplus Z_1 \oplus W_2$$
$$D_2 = X_2 \oplus Y_1 \oplus Z_2 \oplus W_1$$

ii) Parity bits (P1, P2, P3, P4) using XOR operation taking the first bits, second bits, third bits and the fourth bits from four groups

$$P_1 = X_1 \oplus Y_1 \oplus Z_1 \oplus W_1$$
$$P_2 = X_2 \oplus Y_2 \oplus Z_2 \oplus W_2$$

iii) Check bits (Cx, Cy, Cz, Cw) using XOR operation by taking the alternative bits

$$Cx_{13} = X_1 \oplus X_3$$
$$Cx_{24} = X_2 \oplus X_4$$
$$Cy_{13} = Y_1 \oplus Y_3$$
$$Cy_{24} = Y_2 \oplus Y_4$$

3.3Process of decoding

In decoding, the syndrome calculation has been analyzed with the encoded data and the recalculated encoded bits (SDi, SPi and SCi). After that, verification, region selection and correction can be performed.

Figure 3: Different regions of data bits

STEP 4: Calculate the syndrome values for diagonal, parity and check bits by performing XOR operation between the redundancy data stored and the recalculated redundancy bits

$$SD_i = D_i \oplus RD_i$$
$$SP_i = P_i \oplus RP_i$$
$$SC_i = C_i \oplus RC_i$$

where i = 1, 2, 3, 4

STEP 5: Check the following conditions to identify the error that to be satisfied

i) SDi and SPi bits have atleast one value similar to 1

ii) More than one SCi value was similar to 1

STEP 6: Perform region selection and change the erroneous data to get the corrected output.

Divide the data bits into regions 1, 2 and 3. This is formed by dividing the data bits by columns (1&2, 3&4, 2&3) to get efficient results.

4. RESULTS& DISCUSSION

Simulation results provide a comprehensive understanding of how the designed circuit behaves under different conditions. They are crucial for verifying the functionality, identifying and resolving issues, and ensuring that the circuit meets the desired specifications before physical implementation. Figure 4 presents the simulation results of proposed system, where we can detect the error and correct the error .

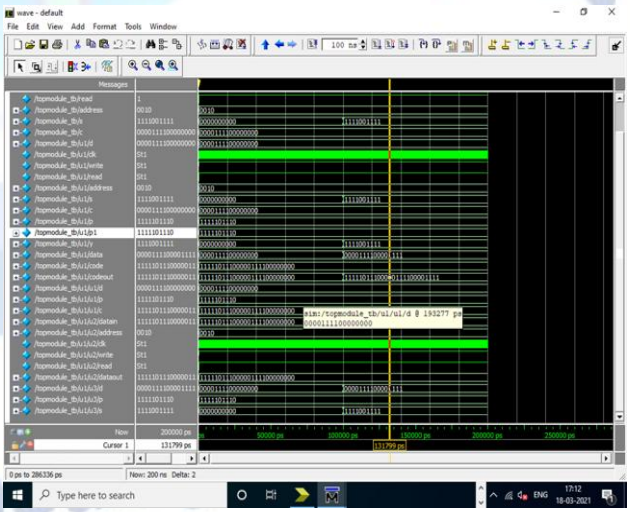

Figure 4: Simulation results of the proposed system

The block diagram offers a high-level representation of the entire system, illustrating the functional blocks and their interconnections. It serves as a visual guide for system architecture, aiding designers in conceptualizing and communicating the design structure and functionality. Figure 5 shows the block diagram of the proposed system.It consists of input

(clk,rst,read,write,address,data in) and output(code word and syndrum) as output.

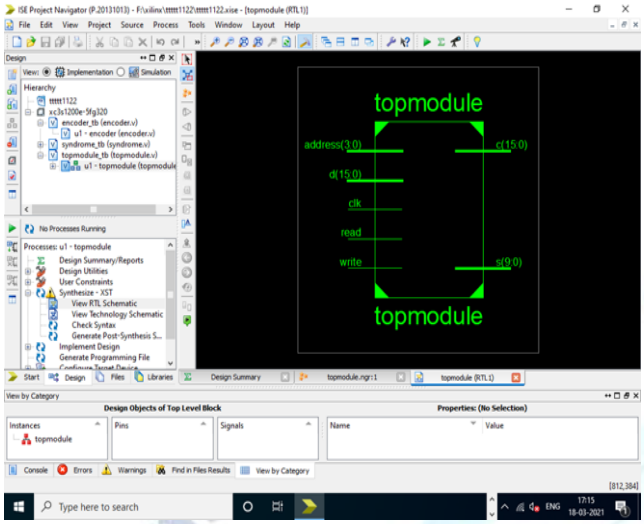

Figure 5: Block diagram of the proposed system

RTL schematics depict the digital logic at a higher abstraction level, showing the flow of data between registers and logic elements. This representation is vital for understanding the data flow within the circuit, facilitating optimization, synthesis, and ensuring proper mapping of the design to hardware. Figure 6 shows the RTL schematic of the proposed system.the RTL which consists of Encoder,Syndrum and Memory.

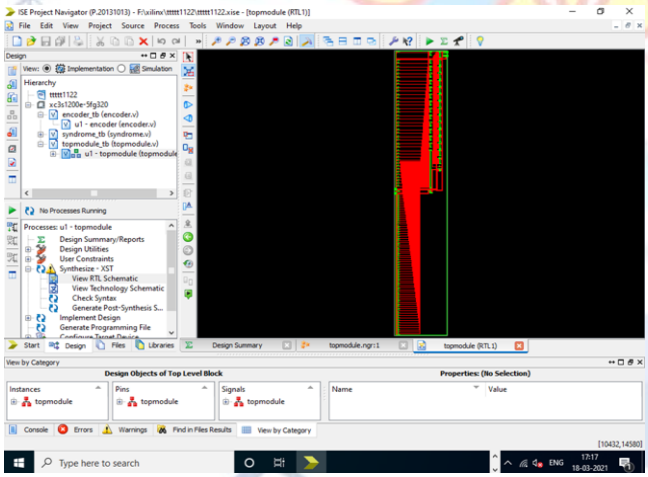

Figure 6: RTL Schematic of the poposed system

Power consumption is a critical consideration in modern VLSI design. Estimating power consumption helps designers optimize the design for power efficiency, which is crucial for battery-operated devices and minimizing environmental impact. Power estimation also guides decisions on cooling mechanisms. Figure 7 presents the power estimation of the proposed system.The power consumed in the circuit is 0.158w.

Delay estimation is essential for ensuring that the designed circuit meets timing requirements. It helps identify and address timing issues such as setup and hold time violations, ensuring that signals propagate through the circuit within the specified time constraints. Figure 8 presents the delay estimation of the proposed system. The delay in the circuit is 2.279ns.

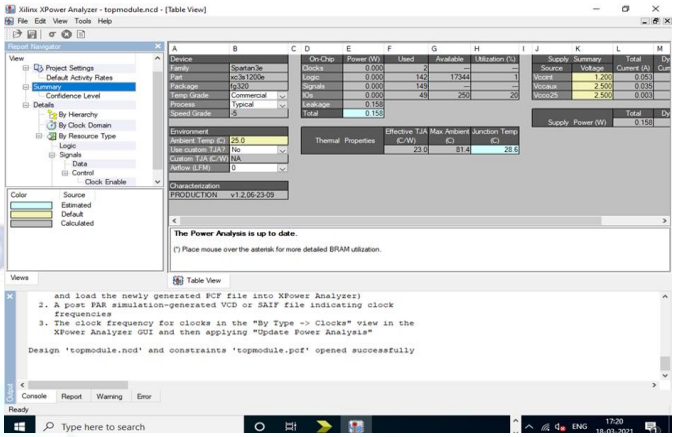

Figure 7: Power estimation of the poposed system

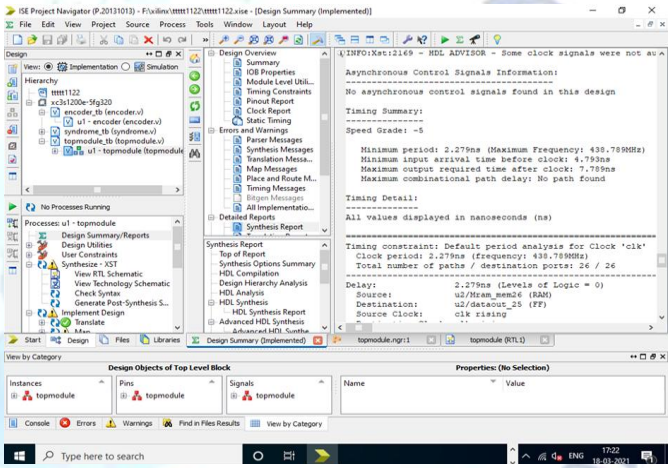

Figure 8: Delay estimation of the poposed system

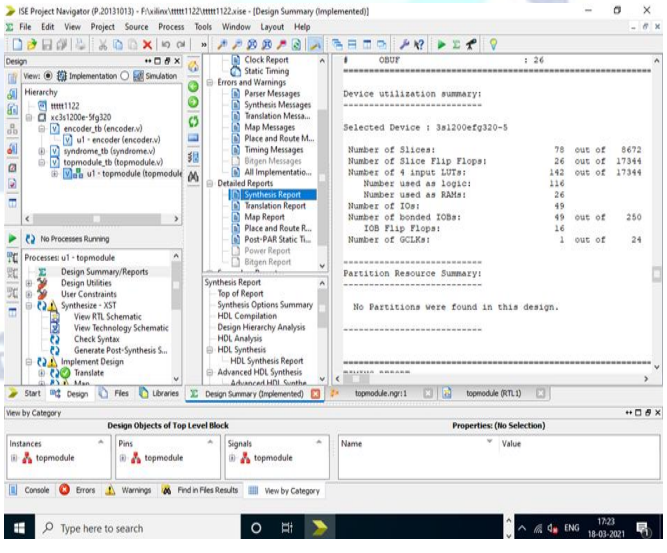

Figure 9: Area estimation of the poposed system

Area estimation provides insights into the physical space occupied by the designed circuit on the semiconductor. It is crucial for optimizing the use of resources and determining the overall size of the chip. Efficient area utilization contributes to cost-effectiveness and manufacturability. Figure 9 presents the area estimation of the proposed system. The area report shows that it contains 142 look up tables.

5. CONCLUSIONS

In this work, a new error correction code (ECC) is proposed to reduce data corruption in volatile memories. The proposed scheme was simulated and synthesized using Xilinx ISE implemented in Verilog HDL. Compared with the well known existing methods, this encoding-decoding process consumes low power and occupies minimum area and delay. Further, this algorithm is to be extended to reduce the area, delay and power consumption. As the regions were selected particularly, the decoder area increases compared to the other existing methods. Further, this is reduced by using the advanced region selection criteria.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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