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A Novel Approach to reduce Energy/Power in a Parallel Decimal Multiplier

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ABSTRACT

Despite the fast and effective implementation of binary arithmetic functions, using decimal computation has been revived. This revitalization has been done for three main reasons; (1) the advances in VLSI technology, (2) the appearance of a large amount of decimal data in human-centric applications such as financial, commercial, scientific, and internet-based applications so that the software implementations. Decimal computation is highly demanded in many human-centric applications such as banking, accounting, tax calculation, and currency conversion. Hence the design and implementation of radix-10 arithmetic units attract the attention of many researchers. Among the basic decimal arithmetic operations, multiplication is not only a frequent operation but also has high complexity and considerable power consumption. Therefore, this paper concentrates on this issue and studies a general design methodology that reduces power/energy consumption via localizing switching activity without compromising target performance. This method decomposes a digit multiplier into smaller ones, like Karatsuba's algorithm, while the multiplicand and the multiplier can be partitioned into different sizes. We take advantage of various size partitions in two types of symmetric and asymmetric, which final designs provide specific characteristics. Evaluation results for 16-digit operands show that the proposed architectures have interesting area-delay figures compared to conventional binary multipliers and outperform the figures of previous alternatives for decimal multiplication. It will be developed using Verilog HDL. Xilinx ISE tool is used to perform the Simulation and Synthesis.

Keywords: Decimal computation, digital arithmetic, low power design, parallel multiplier

1. INTRODUCTION

Despite the fast and effective implementation of binary arithmetic functions, using decimal computation has been revived. This revitalization has been done for three main reasons; (1) the advances in VLSI technology, (2) the appearance of a large amount of decimal data in human-centric applications such as financial, commercial, scientific, and internet-based applications so that the software implementations do not satisfy the high-performance requirements [1], and finally (3) the lack of exact binary representation for some decimal fractions (e.g., 0.2). The former made hardware realization of complex functions possible, while the two others pushed the designers to use

hardware-implemented decimal arithmetic units for coping with the complexity of processing a massive amount of data with acceptable precision and time. Due to the importance of decimal arithmetic, the new feature of decimal representation and related operations is added to the latest revision of IEEE 754 standard for Floatingpoint arithmetic [2], [3]. Moreover, concerted activity in both industry and academia is progressing on decimal arithmetic. Several processors have been announced, such as IBM eServer z900 [4], IBM POWER6 [5], and IBM z10 [6], which are equipped with a dedicated decimal arithmetic unit. On the other hand, a considerable number of research papers have been published on decimal arithmetic algorithms and hardware units such as decimal addition [twooperand (e.g., [7]) and multi-operand (e.g., [8])], decimal multiplication [sequential (e.g., [9]) and parallel (e.g., [10])], decimal division [subtractive (e.g., [11]) and multiplicative (e.g., [12])], and other arithmetic functions (e.g., [13]). Among various operations, decimal multiplication is known as one of the most complex operations, which is high frequency, time-consuming, and power-hungry. In addition, it is iteratively used to implement other useful operations such as division, square root, and function evaluation circuits like radix-10 exponentiation and logarithm. Hence, high-speed decimal multiplication takes particular attention, and severalpublications have been published on this topic in less than ten years. The proposed methods of these articles are focused on latency and area as the main design parameters, while the power/energy consumption is neglected. Whereas, the cooling issue in high-performance processing systems and the limited power budget in embedded systems, as well as the effects of consumed power in the efficiency and reliability of digital circuits, make the power/energy consumption the most challenging parameter for nowadays hardware designers [14]. In [15], we provide a comparative study on the leakage and dynamic power consumption of released high-speed decimal multipliers and suggest some guidelines for EDA tools and hardware designers. In this paper, we target to reduce power/energy consumption in high-speed decimal multipliers (i.e., parallel decimal multipliers). To achieve the best result, we use the highest level of design abstraction for applying power reduction techniques, since power optimizations at the higher levels of design abstraction have the maximum influence. Our suggested method is based on partitioning (like Karatsuba's algorithm) and reduces power/energy consumption by localizing switching activity without any negative impact on performance. In our proposed method, we implement a digit multiplier (i.e., IEEE 754-2008 standard) via smaller ones in two different types of symmetric and asymmetric. In symmetric designs, all smaller multiplier units have the same size, while different sizes of multipliers may be used in asymmetric ones.

2. EXISTING MULTIPLICATION APPROACH

The concept of the carry-select adder is to compute alternative results in parallel and subsequently selecting the correct result with single or multiple stages. In carry-selectadders both sum and carry bits are calculated for the two alternatives: carry 0 and 1. Once the carry-in is fired, the correct computation is chosen using multiplexers to produce the desired output. Therefore, instead of waiting for the carry-in to calculate the sum, the sum is correctly output as soon as the carry-in gets there. The time taken to compute the sum is then avoided which results in a good improvement in speed.

Here, four 4X4 Vedic multiplier blocks and three carry select adders of 8 bits each are used. The arrangement of the carry select adders is made in a different way such that it requires less computation time. Some of the carry select adders are given with zero inputs, wherever required. The output of middle multipliers is added using first CSLA. The Output of first CSLA and first Vedic multiplier are added using second CSLA. Carry outputs from first two CSLAs are performed by OR operation and it is given as an input to the third CSLA to generate the final result.

The design of 16×16 block is a similar arrangement of 8×8 blocks in an optimized manner which is shown in Figure 1. The first step in the design of 16×16 block will be grouping the 8 bit (byte) of each 16-bit input.The LSB of two inputs will form vertical and crosswise product terms.Each input byte is handled by a separate 8×8 Vedic multiplier to produce sixteen partial product rows. These partial products rows are added in a 16-bit carry select adder optimally to generate final product bits. The schematic of a 16×16 block is designed by using the 8X8 Vedic multiplier. The partial products represent the Urdhva vertical and cross product terms. Then by using or gate, the final product is obtained.

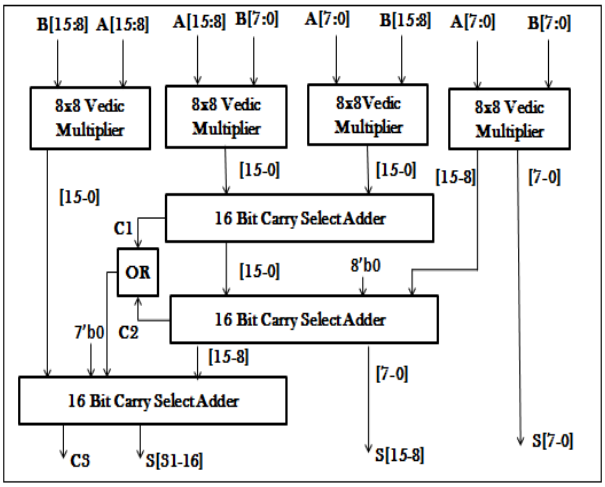


Figure 1: Block Diagram of 16X16 bit Vedic Multiplier

The use of carry select adder increases the hardware thereby more power consumption which is twice that of rippe carry adder.The use of multiplexer increases the chip area.But considerable increase in the speed is achieved. So, optimization of the carry select adder can beuseful inincreasing the speed of the multiplier.

3.PROPOSED MODEL

The Karatsuba algorithm is a well-known technique for reducing the delay of large numbers multiplication which is based on divide and conquer. According to this algorithm, several high-speed multipliers have been proposed. However, this paper focuses on power reduction of decimal multiplication via partitioning, like the Karatsuba technique. It uses smaller multipliers (i.e., multiplier cells) and provides appropriate granularity for localizing switching activity. Nevertheless, some issues like the size of utilized multiplier cells and the basic multiplication algorithm should be studied carefully.

3.1 Decimal Multiplication Via Partitioning

As mentioned above, the Karatsuba algorithm, via divide and conquer, accelerates the multiplication of large numbers. It was originally implemented for binary multiplication. Based on this algorithm in decimal multiplication, for computing $P = X \times Y$ the operands can be recursively divided into two partXH, XL and YH, YL, respectively. In this regard, XH and YH show the most significant parts, while XL and YL demonstrate the least significant portions. Thus, by assuming $k = 2n$ and equal partitioning, the operands can be rewritten in the form of Equation (2).

$$X = 10^n \sum_{i=0}^{n-1} x_{i+n} 10^i + \sum_{i=0}^{n-1} x_i 10^i = X_H 10^n + X_L$$
$$Y = 10^n \sum_{i=0}^{n-1} y_{i+n} 10^i + \sum_{i=0}^{n-1} y_i 10^i = Y_H 10^n + Y_L \quad (2)$$

After partitioning, based on the Karatsuba multiplication algorithm, the P D X x Y product is constructed by Equation (3).

$$P = (X_H 10^n + X_L)(Y_H 10^n + Y_L)$$
$$= 10^{2n} X_H Y_H + 10^n (X_H Y_L + X_L Y_H) + Y_L Y_L \quad (3)$$

Implementation of Equation (3) needs four nX$n$digit decimal multiplications and two $2n$-digit and $3n$-digit additions. This algorithm can be recursively continued till it achieves to 1X1 digit multiplication.

3.2 Symmetric Approach

For symmetric designs, we consider three different partitioning sizes of operands, namely, two, four, and eight. In the first design, multiplier and multiplicand are partitioned into two equal parts, so four 8 X 8 -digit multipliers are used to create a 16 X 16 -digit multiplier according to Equation (3).The output of multiplier cells must be aligned before the final reduction and conversion steps. This alignment is shown in Figure 1, where the eight bits of the least significant part, without any extra computation, form the least significant part of the final result. However, the 8th to 23rd positions need a multi-operand addition. Also, an increment operation is required for the eight bits of the most significant part (increment with carry out of multi-operand addition). It should be mentioned that the algorithm of multiplier cells is essential since it has a significant impact on the detail design and low-level architecture of the main multiplier. Thus, the discussion about the multiplier cells and the related influential characteristics of the algorithm

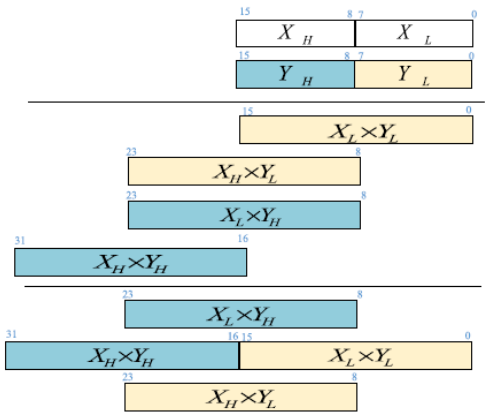


Figure2: The arrangement of the 16 X 16-digit multiplier by four 8 X 8 multipliers (mult.16-8)

The idea of divide and conquer can recursively be used to implement each multiplier cell with smaller ones. For example, a 4*n* X 4*n*-digit multiplier needs four 2*n* X 2*n*-digit multipliers, as mentioned above. By more partitioning, each 2*n* X 2*n*-digit multipliers can be implemented via four *n* X *n*-digit multipliers. According to these explanations, we can implement a 16 X 16-digit multiplier by using sixteen 4 X 4-digit multipliers, as shown in Figure 3.

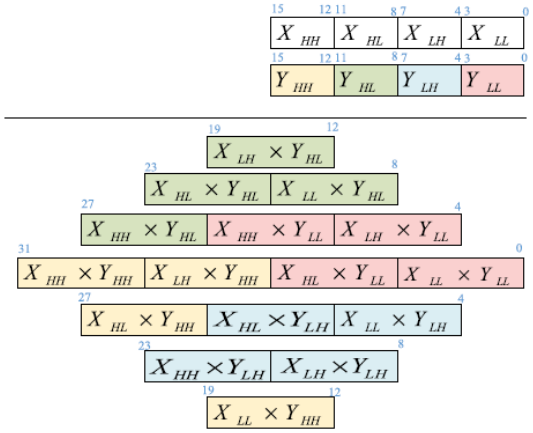


Figure3: The arrangement of the 16 X 16-digit multiplier by sixteen 4 X 4-digit multipliers (mult16-4)

The extreme point of partitioning provides a parallel multiplier which its partial products generate via digit-by digit multipliers. Since all the state-of-the-art multipliers use pre-computed multiplies (based on background information), we define the 2X2-digit multiplier as the smallest multiplier cell. According to this definition, we can partition operands into eight equal parts and construct a 16X16-digit multiplier by using sixty-four 2_2-digit multipliers, as shown in Figure 4.

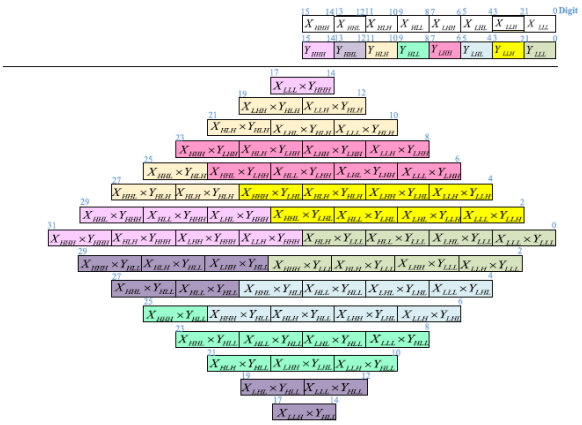


Figure 4: The arrangement of the 16 X 16-digit multiplier by sixty-four 2 _ 2-digit multipliers

By reviewing the aforementioned architectures, two important issues should be considered. The first is the depth of the multi-operand adder, and the second is the output format of multiplier cells. The depth of the multi-operand adder in Fig. 3, 4, and 5 are 3, 7, and 15, respectively. Obviously, using smaller multiplier cells provides more granularity. However, it increases the area consumption. So, a detailed analysis with power dissipation monitoring is required to compromise the size of multiplier cells and area consumption. To address the second issue, based on Fig. 2, the output of multiplier cells is in BCD format, which is provided after a redundant to non-redundant conversion. It causes an unnecessary time-consuming carry propagation that can be omitted since the output of multiplier cells feed to a multi-operand adder. Of course, this adder has to accept redundant inputs. This issue is related to the algorithm of multiplier cells.

3.3 Asymmetric Approach

As mentioned before, different sizes of multiplier cells are possible. Although the bigger multiplier cell has more delay, it may increase the total delay of the main multiplier due to imbalance delay paths. Moreover, an asymmetric method can show considerable superiority for an input pattern with special statistical properties (The experimental results are provided in Section 5). Since possible partitioning for asymmetric design is many, this category's advantage is shown by studying just a straightforward partitioning to illustrate a specific pattern of power consumption in our proposed method.

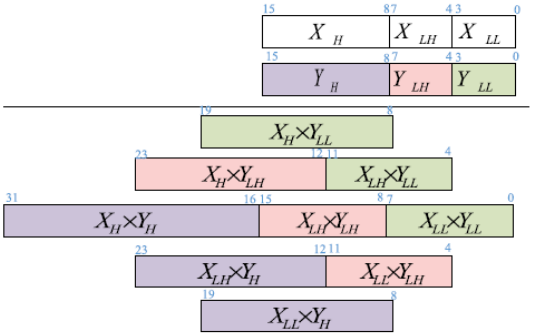


Figure5: The arrangement of the 16 X 16-digit multiplier with asymmetric partitioning (mult16-8-4)

In Figure 5, the arrangement of the 16_16-digit multiplier is shown, which is partitioned asymmetrically. This multiplier is composed of various multiplier cells (i.e., four 4 X 4- digit multipliers, two 4 X 8-digit multipliers, two 8 X 4-digit multipliers, and one 8 X8-digit multiplier).

3.4 Ripple Carry Adder (RCA)

Ripple Carry Adder is a basic adder circuit which contains individual full adder cells and the carry generated upon addition is propagated between the respective adder cells. The computation of result takes place only after the carry from the previous stage is applied as an input to present stage. Due to these propagation delays, the delay is bound to occur which is a major disadvantage. The architecture of the 32-bit RCA is shown in Figure 6.

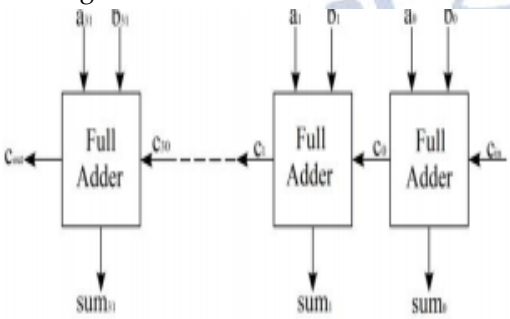
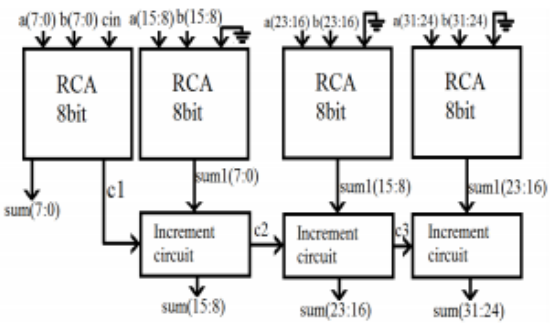


Fig.5 32-bit ripple carry adder

Figure 6: 32-bit RCA

3.5 Compute Add Increment (CAI) adder

In CAI adder, various RCA blocks are used to compute the results. The first RCA block is given carry-in as input along with addends to get carry(c1) and sum. For the rest RCA blocks, the carry-in is given as logic ⊚0⊚ to get temporary sum (sum1) and temporary carry which are given to increment circuit. Increment circuit consists of half adders which add temporary sum and carries to get the actual sum(sum) and carry (cy). The carry-out of increment circuit is obtained by performing OR operation between carry (cy) and carry-out of the previous stage. As the carry-in for the RCA stages is logic ⊚0⊚ and hence the carry propagation delay decreases. The architecture for the CAI 32bit is shown below.



4. RESULTS& DISCUSSION

Simulation results provide a comprehensive understanding of how the designed circuit behaves under different conditions. They are crucial for verifying the functionality, identifying and resolving issues, and ensuring that the circuit meets the desired specifications before physical implementation. Figure 7shows the simulation wave of the proposed multiplier.

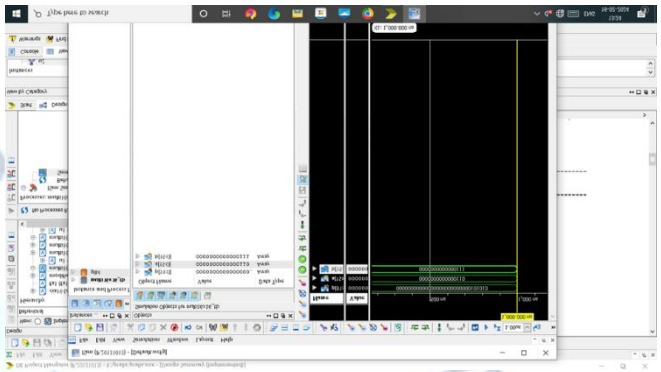


Figure 7: Simulation results of the proposed multiplier

The block diagram offers a high-level representation of the entire system, illustrating the functional blocks and their interconnections. It serves as a visual guide for system architecture, aiding designers in conceptualizing and communicating the design structure and functionality. Figure 8 shows the block diagram of the proposed multiplier.

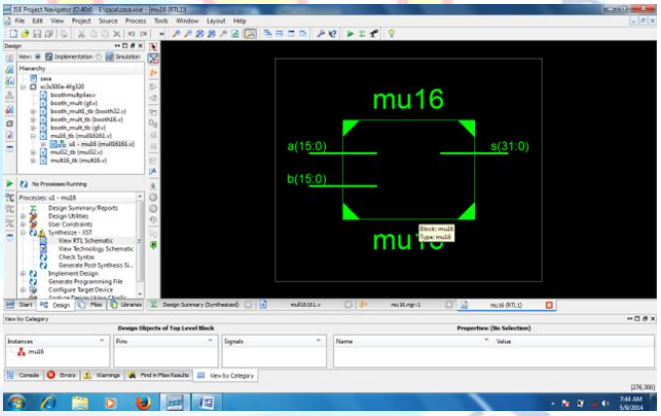


Figure 8: Block diagram of the proposed multiplier

RTL schematics depict the digital logic at a higher abstraction level, showing the flow of data between registers and logic elements. This representation is vital for understanding the data flow within the circuit, facilitating optimization, synthesis, and ensuring proper mapping of the design to hardware. Figure 9 shows the RTL schematic of the proposed multiplier.

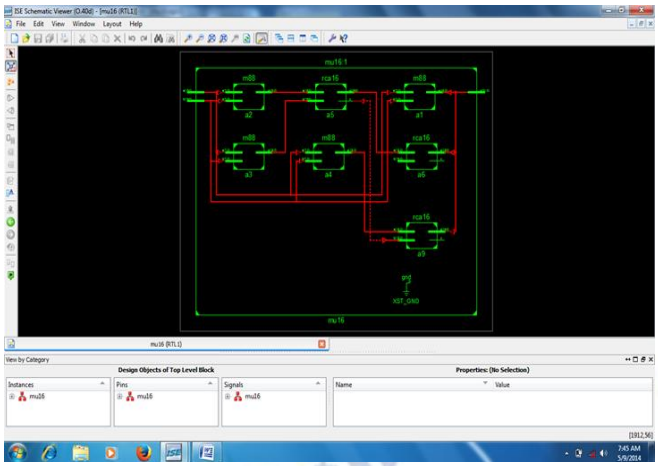


Figure 9: RTL Schematic of the poposed system

It shows the multiplier circuits and adders. Power consumption is a critical consideration in modern VLSI design. Estimating power consumption helps designers optimize the design for power efficiency, which is crucial for battery-operated devices and minimizing environmental impact. Power estimation also guides decisions on cooling mechanisms. Figure 10 presents the power estimation of the proposed system.The power consumed in the circuit is 0.368w.

Delay estimation is essential for ensuring that the designed circuit meets timing requirements. It helps identify and address timing issues such as setup and hold time violations, ensuring that signals propagate through the circuit within the specified time constraints. Figure 11 presents the delay estimation of the proposed system. The delay in the circuit is 42.24 ns.

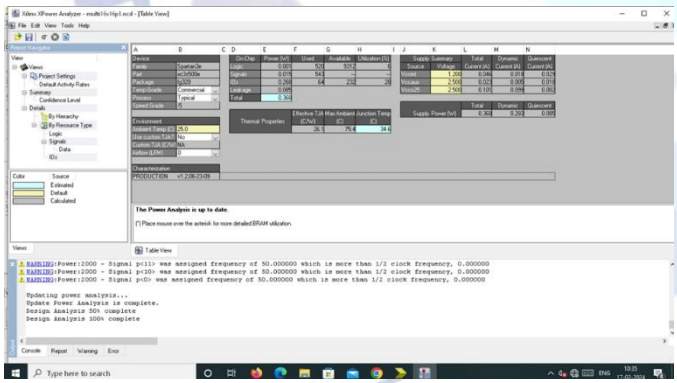


Figure 10: Power estimation of the proposed multiplier

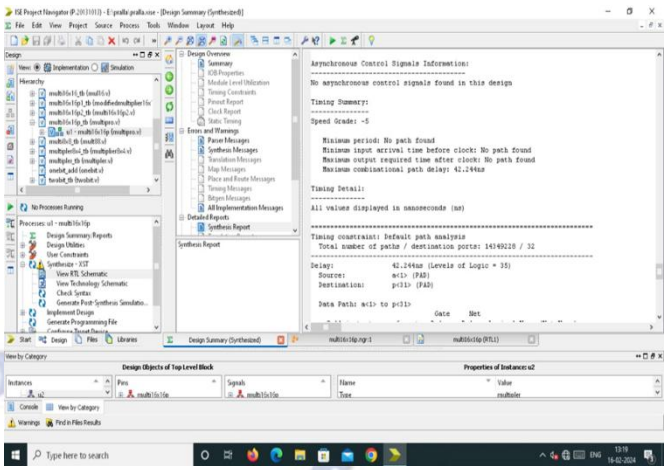


Figure 11:Delay estimation of the proposed Multiplier

Area estimation provides insights into the physical space occupied by the designed circuit on the semiconductor. It is crucial for optimizing the use of resources and determining the overall size of the chip. Efficient area utilization contributes to cost-effectiveness and manufacturability. Figure 12 presents the area estimation of the proposed system. The area report shows that it contains 644 look up tables.

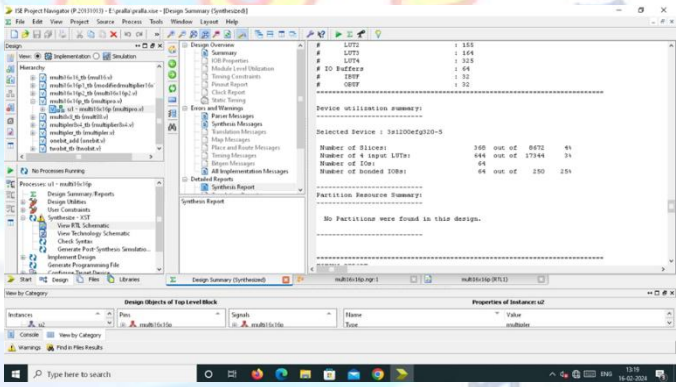


Figure 12: Device utilization summaryof the proposed multiplier

5. CONCLUSIONS

Due to the importance of decimal computation, in this paper, we study a design methodology for reducing the power consumption of decimal multipliers. The suggested method is based on partitioning, which constructs a large multiplier with the smaller ones. The proposed architectures and the original multiplier (which are used as multiplier cells) were implemented via structural Verilog and synthesized with Xilinx ise.

The experimental results demonstrate delay reduction when all the input signals are active.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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