International Journal for Modern Trends in Science and Technology
Volume 10, Issue 02, pages 388-393.
ISSN: 2455-3778 online
Available online at: http://www.ijmtst.com/vol10issue02.html
DOI: https://doi.org/10.46501/IJMTST1002051

Xilinx-Enhanced Electronic Voting Machine with Advanced Security Features

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To Cite this Article
Raju Thommandru, Sanka Deekshitha, Sireesha Adapa, Pasala Sarath Babu, Mohammad Riyaz Pashi, Xilinx-Enhanced Electronic Voting Machine with Advanced Security Features, International Journal for Modern Trends in Science and Technology, 2024, 10(02), pages. 388-393.https://doi.org/10.46501/IJMTST1002051

Article Info
Received: 30 January 2024; Accepted: 21 February 2024; Published: 26 February 2024.

ABSTRACT

This work addresses the challenges faced by closed spaces, such as shopping malls and multistoried buildings, in efficiently managing parking slots and minimizing manual labor. The primary objective is to develop a sophisticated parking system with multiple slots, alleviating issues related to tight parking spaces and the substantial manual effort required for space tracking within confined areas. The core focus revolves around designing a smart car parking system implemented using Verilog. The system incorporates a sensor at the entrance to detect the presence of a vehicle. Upon sensor activation, a password is prompted for gate access. If the entered password is accurate, the gate opens, granting entry to the vehicle; otherwise, the gate remains securely locked. This innovative solution aims to streamline parking management, enhance security, and reduce the manual workload associated with monitoring parking spaces in enclosed environments.

Keywords: Parking System, Verilog Implementation, Sensor-based Access, Smart Parking, Manual Labor Reduction

1. INTRODUCTION

The proposed work by [4] outlines a decentralized 3-layer control architecture that incorporates authority management, voting, and linkable ring signatures. This architectural design aims to strike a balance between the efficiency of the voting system and control over the number of proxy nodes, ultimately enhancing ballot privacy. In a similar vein, [5] introduces a secure e-voting system featuring a crypted database (DB) with data storage in the cloud. This approach ensures secure data analysis, computation, and integrity during the voting process, allowing for the tracing of intruders and preventing malicious administration. Emphasizing confidentiality, data security, and process integrity, [6] introduces a sophisticated approach to student employment counting, leveraging multilayer perceptron with Bayesian methods, random forest, decision trees, and ML algorithms such as J48. Furthermore, [7] proposes an internet e-voting method that fulfills requirements such as validity, confidentiality, and integrity, incorporating blind signature methods to counter rigging in elections. Lastly, [8] presents a blockchain-based approach for e-governance and e-voting, adopting an exploratory and qualitative methodology for peace engineering.

2. LITERATURE REVIEW

In [1], authors have introduced a digital nature password system. It is simulated in Xilinx and helps in replacing the paper ballot system and gives a memory efficient method. In this method, more number of votes can be casted in minimum time and storing of votes becomes easy as it is digital system and password is also a protective method for the whole process to take place in an effective way. In [2], authors have introduced an electronic voting machine which involves 3- stages in voting process. First step is venable to start the voting, second step is to collect the votes of contestants and third step is counting and declaring the results. It is a digital process with random password to the voter. This makes the process easy, secure and safe. It also reduces the ballot paper method complexity and storage of votes is digital and more confidential [15], [16]. A hybrid structure with bloom filter, merkle hash tree involved in block chain for electronic e-voting is contributed by [3]. It helps in high efficiency and low overhead which in turn useful for large-scale e-voting systems. In [9], authors have given an overview of voting system in various countries. International level of analysis is done to identify the loop holes in e-voting systems. The main idea is to authenticate the voters and secure the system form miscreants. Open voting consortium is proposed by [10]. It helps in recording process in voting system and gives voter privacy, ballot secrecy. It also plays major role in political culture of partial or complete privacy in voting system. Aadhar based voting system is proposed by [11]. It is designed in arduino and provides security and privacy in voting process of online electoral voting system for elections in India. An electronic voting machine is designed by [12] which is microcontroller based and helps in improving secure and privacy in democratic voting system particularly in Bangladesh. Cost analysis is carried out for the implemented electronic voting system to check its better performance. An electronicvoting machine based on finger print and arm9 microcontroller is proposed by [13]. It is user friendly and cost effective thereby supports digital recording, storing and processing in electronic voting system. Arduino based smart voting system is designed by [14]. Based on biometric finger print, voter will be allowed to cast the vote and display on LCD gives transparency of voting to the voter and the electronic voting system.

3.SECURITY BASED ELECTRONIC VOTING MACHINE

Electronic voting machine plays major role in democratic society for voting system to avoid rigging. For giving privacy for voters and secure, integrity in elections and counting of votes and to avoid age old ballot papers in voting process electronic voting machines are highly necessary. In our work, voting process is considered with 3 contestants namely party0, party1, party2 and seg0, seg1, seg2 are registers to store the votes of party0, party1, party2 respectively. Venable is used to enable voting process and clk is used to enable the entire election process. Vswitch is a 2-bit input which can be used to activate the voting for each contestant respectively. If vswitch is 00, then voters can vote for party0, if Vswitch is 01, then voters can vote for party1 and if Vswitch is 10, then voters can vote for party2. Dout will hold the total votes of all contestants, invalid is the signal that gets activated when Venable is not in high state to start the voting process and if voter tries to vote for any contestant. Security can be incorporated by OTP generation and verification of it from the voter's mobile before allowing the voter for voting process. A pseudo random binary sequence generator (PRBS) can be used to generate a 6-bit random number which can be used as OTP. Hence, the entire process of digital electronic voting system may help in a safe, secure and integrity process in a democratic society.

The OTP for the above applications are generated by Linear Feedback Shift Register (LFSR). The 8-bit pattern generation circuit to generate a pattern X^7+X^5 +X^4+X^3+1 is shown in Figure 1. As the technology advances, the need for low power consumption circuit increases. Thus, the circuit is generally expected to be designed in such a way that it should consume less power, occupy minimum area with improved response time. The use of flip-flop with activated clock in the register design consumes more power which is not sufficient for high throughput, so pulsed latches are used in the place of flip-flops in this proposed work. For reducing the power consumption of the device, various methodologies are available in the literature. Dropping the number of transitions is one of the means for power optimization.

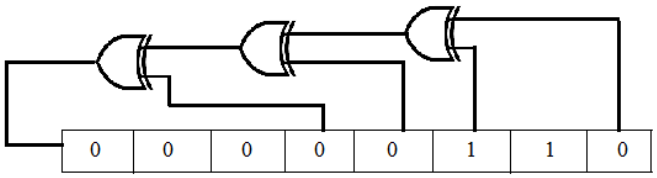

Figure 1: 8-bit LFSR architecture and output

For reducing the power consumption of the device, various methodologies are available in the literature. Dropping the number of transitions is one of the means for power optimization. Transitions are reduced by swapping the bits and applying clock to half part of the circuit. Clock gating is also employed for power optimization. Although various optimization techniques are implemented for minimizing the power consumption of the device, they are not eventually much effective by the means of reducing the response time and area. Like power optimization techniques, techniques for minimizing the area and increasing the speed are also employed in [1]-[5]. The conventional method of serial to parallel architecture and pipelining algorithms are used to increase the speed of the shift register. Also calculation of output value only by considering the past feedback value in the transposed serial architecture, increases the speed. The transformation from long LFSR sequence to several short LFSR sequence in series reduces the overhead. Though several techniques are used to reduce the power, area and speed, they are not efficient in terms of critical path delay.

LFSR is a serially connected flip-flop configuration – shift register configuration – with feedbacks from certain flip-flop outputs – taps – that are XORed together –added in modulo 2 – and connect back to first flip-flop's input. The number and position of taps determine the length and sequence of generated PRBS pattern. An exemplary 8 stage LFSR with tap connections that provide maximum possible sequence length (2n-1 patterns) CA structure is quite similar to that of LFSR, with the inherent shift register configuration. The basic difference from the LFSR is, the interconnections of individual flip Testing and flops now always include an XOR operation and there is no global feedback. CA consist of 2 types of primary cells, namely 90 and 150 cells, and certain combination of these cells reveal maximum length sequences. The only difference between 90 and 150 cells is, 150 cells have an additional self feedback from the flip-flop output to back to its input. An exemplary 4 stage CA, with appropriate 90 and 150 cell configuration for maximum length PRBS.

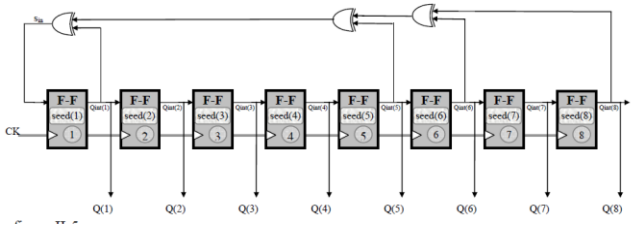

Figure 2: An 8 stage maximum length LFSR

The pseudorandom number generator has the following disadvantages:

- When few bits of the plain text and their corresponding ciphertext are known, then it is easy to hack the data by creating the remaining bits in the key sequence.
- It leads to less security.

4. RESULTS& DISCUSSION

Simulation results provide a comprehensive understanding of how the designed circuit behaves under different conditions. They are crucial for verifying the functionality, identifying and resolving issues, and ensuring that the circuit meets the desired specifications before physical implementation. Figure 3shows the simulation results of proposed voting system.The simulation of the electronic voting machine is depicted, wherein the clock signal initiates the election process, Venable facilitates the voting process, and the V switch is utilized to select the candidate for whom the vote is cast. The outputs, including contestant-specific displays (seg0, seg1, seg2), as well as the total votes (Dout), are generated based on the selected candidate.

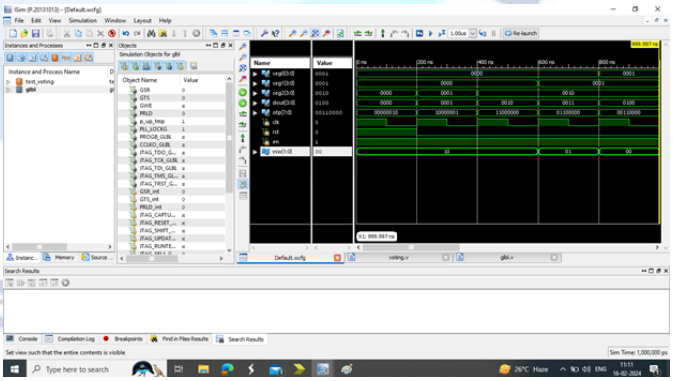

Figure 3: Simulation results of the proposed voting system

The block diagram offers a high-level representation of the entire system, illustrating the functional blocks and their interconnections. It serves as a visual guide for system architecture, aiding designers in conceptualizing

and communicating the design structure and functionality. Figure 4 shows the block diagram of the parking system.The block diagram of the electronic voting machine is illustrated, featuring inputs such as clock, reset, V switch, and V enable. The outputs generated from this system include seg0, seg1, seg2, and Dout.

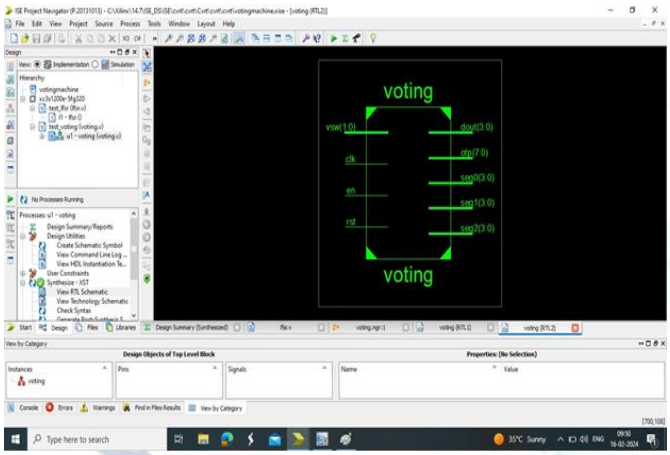

Figure 4: Block diagram of the proposed system

RTL schematics depict the digital logic at a higher abstraction level, showing the flow of data between registers and logic elements. This representation is vital for understanding the data flow within the circuit, facilitating optimization, synthesis, and ensuring proper mapping of the design to hardware. Figure 5 shows the RTL schematic of the proposed parking system.The RTL schematic of the electronic voting machine is presented, revealing the generation of internal circuits within the system.

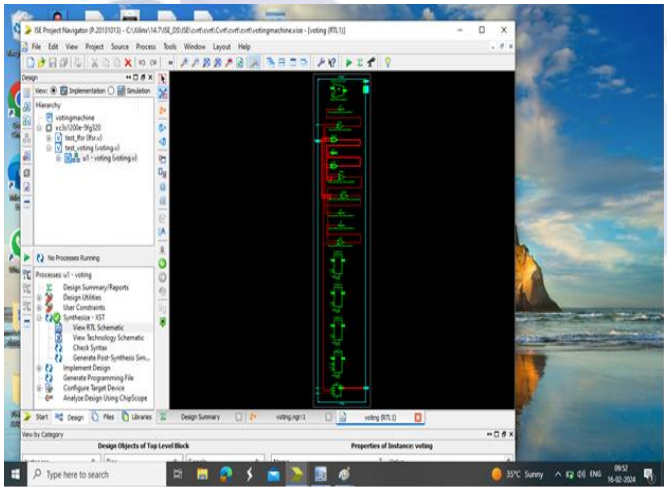

Figure 5: RTL Schematic of the proposed system

Power consumption is a critical consideration in modern VLSI design. Estimating power consumption helps designers optimize the design for power efficiency, which is crucial for battery-operated devices and minimizing environmental impact. Power estimation also guides decisions on cooling mechanisms. Figure 6presents the power estimation of the proposed system.The power consumed in the circuit is 0.108w.

Delay estimation is essential for ensuring that the designed circuit meets timing requirements. It helps identify and address timing issues such as setup and hold time violations, ensuring that signals propagate through the circuit within the specified time constraints. Figure 7 presents the delay estimation of the proposed system. The delay in the circuit is 2.019ns.

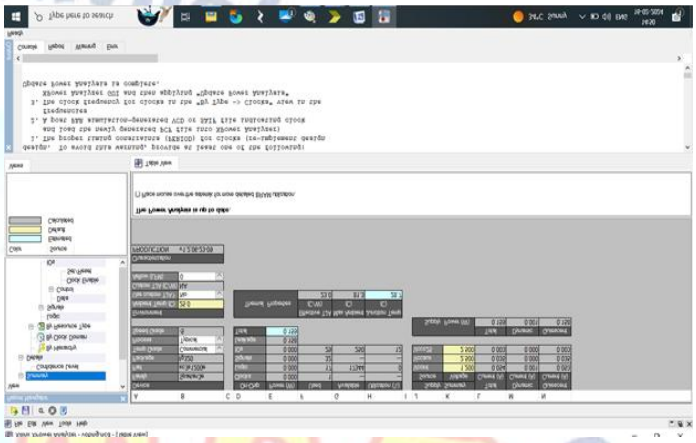

Figure 6: Power estimation of the proposed system

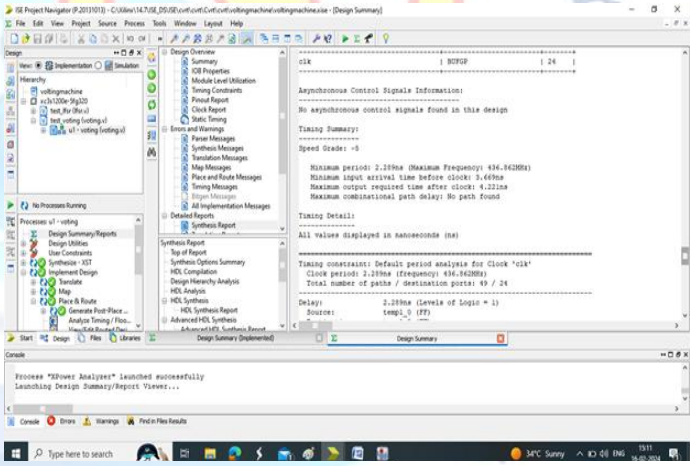

Figure 7: Delay estimation of the proposed system

Area estimation provides insights into the physical space occupied by the designed circuit on the semiconductor. It is crucial for optimizing the use of resources and determining the overall size of the chip. Efficient area utilization contributes to cost-effectiveness and manufacturability. Figure 8 presents the area estimation of the proposed system.

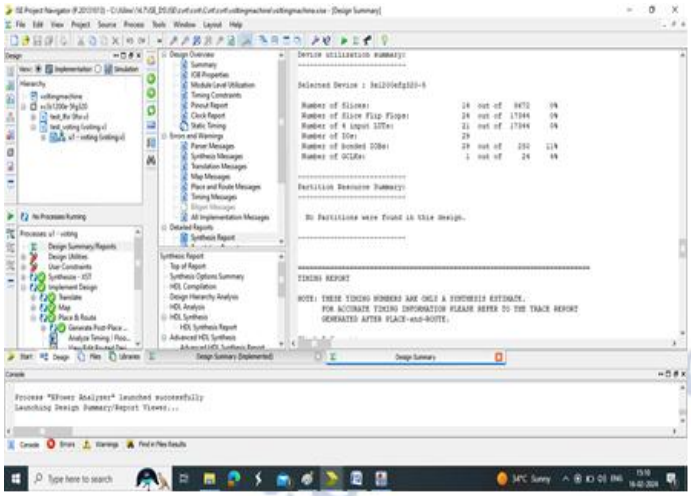

Figure 8: Device utilization summaryof the proposed votingsystem

5. CONCLUSIONS

Electronic voting machines are primary for elections in college level, panchayat or state, country and international levels to maintain integrity in the entire process. We have considered 3 contestants and their voters are stored in separate registers and the total votes for all contestants are also counted and stored for final analysis in the election system. Security can be provided using a 6-bit OTP generation process using pseudo random binary sequence generator. Thus, the process provides a privacy for voters, safe and secure conduction of elections in all levels.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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