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# Design and Analysis of 1-bit Full Adder using Different XOR/XNOR Gates with Mentor Graphics

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## ABSTRACT

*In this paper, a 1-bit Full Adder is designed using different XOR/XNOR gates with Mentor Graphics. A Full Adder is implemented using these XOR/XNOR circuits along with a multiplexer. The designed circuits provide full swing voltage and reduces delay as well as power by comparing with 180nm, 130nm, 90nm, 45nm technologies*

**KEYWORDS:** *XOR-XNOR, Multiplexer, Low Power, Full Adder, Hybrid style*



## I. INTRODUCTION

Now-a-days electronic systems are playing animportant role in our day to day life. The requirement of these system is less power and great performance. To perform these factors digital processing circuits are needed. Therefore, low power has become the primary factor to design digital circuits.The XOR-XNOR circuits are the building blocks in different circuits such as arithmetic circuits, Multipliers, comparators etc. The Full Adder circuit can be designed using hybrid logic style XOR/XNOR circuits to improve the performance. The full adder circuit can beclassified into three sections. First sectiondeals with XOR and XNOR logic generation and second section deals with sum generation and third section deals with carry generation. A multiplexer circuit is used in full adder for sum and carry generation.

In VLSI, the trade-off factors are power and delay, speed, cost. Each circuit has its own advantages and disadvantages depending on the power and delay.

This paper is classified as follows: Overview of XOR/XNOR circuits was discussed in II, Implementation of 1-bitFull Adder circuit was discussed in III. Simulation setupwas discussed in IV and Conclusion was discussed in V.

## II. OVERVIEW OF XOR – XNOR CIRCUITS

Different XOR/XNOR circuits are designed to performdifferentlogic style full adders. The important factors are full swing and concurrent generation of XOR/XNOR output to reducedelay as well as power consumption.

The XOR/XNOR gate circuit, using double pass-transistor logic (DPL) style, is represented in the Fig.1(a). In this full swing operation is achieved bycombining PMOS in parallel with NMOS, but increases power consumption. The size of transistors also increases due to the presence of NOT gate which is connected to drive the output load.

The XOR/XNOR circuit is designed using transmission gate (TG) and pass-transistor logic (PTL) style asrepresented in Fig.1. (b). It isperformed using ten number of transistors along with one inverter. The inverter is used to invert the input signal. Due to presence of inverter it leads to further increase in the delay and power consumption.

The delay is reduced in XOR-XNOR, Concurrent output circuits are designed. These Concurrent XOR-XNOR circuit uses two inverted signals which are taken from the output load. Thus, it reduces delay.

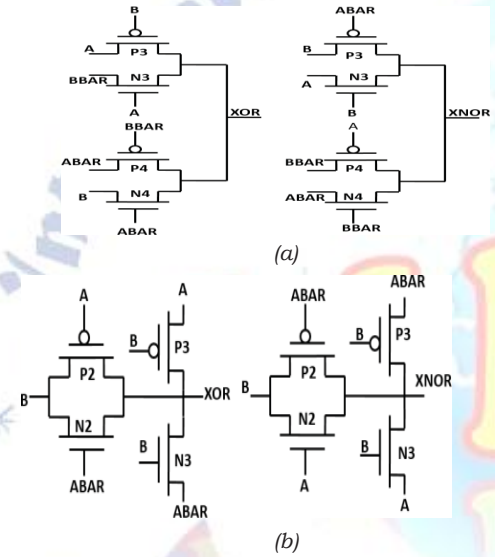


*Fig1.(a)-(b) XOR/XNOR circuit with Full Swing operation*

The Fig.2 (a) represents theconcurrentoutput of XOR–XNOR logic circuit using complementary pass-transistor logic (CPL) style. It implements a logic gate where each gate consists of NMOS-only pass transistors followed by two PMOS transistors. The PMOS transistors are cross coupled at the output. Due to cross coupling of PMOStransistors the power increases. Therefore, it reduces delay and size of transistors increases.

The altered structure of Fig.2 (a) is shown in theFig.2 (b). In this XOR– XNOR circuit is designed by reducing an inverter, which decreases power consumption. In this short circuit current dominates and also, proper sizing is necessary.

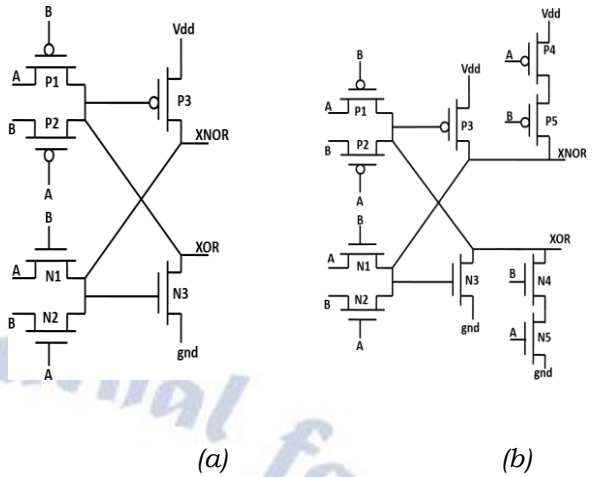


*Fig 2. (a)-(b)Concurrent output of XOR/XNOR logic circuit*

The Full Swing XOR/XNOR logic circuit is shown in Fig.3 (a) shows full-swing XOR–XNOR gate using six transistors. N3 and P3 are two Complementary feedback transistors which restores the weak logic in output terminals, when two inputs are same. It has more delay. The problem of this circuit is the slow response increases for low voltage operation.

There is an improvement in full swingin Fig.3 (b) compared to Fig.3 (a)structure. The delay problem is eliminated by adding two NMOS and PMOS at the output terminals.

Compared to Fig.3 (b) structure Fig.3(c)having a smaller number of transistors, which increases the speed of the circuit. Due to the presence of NOT gate power consumption increases.

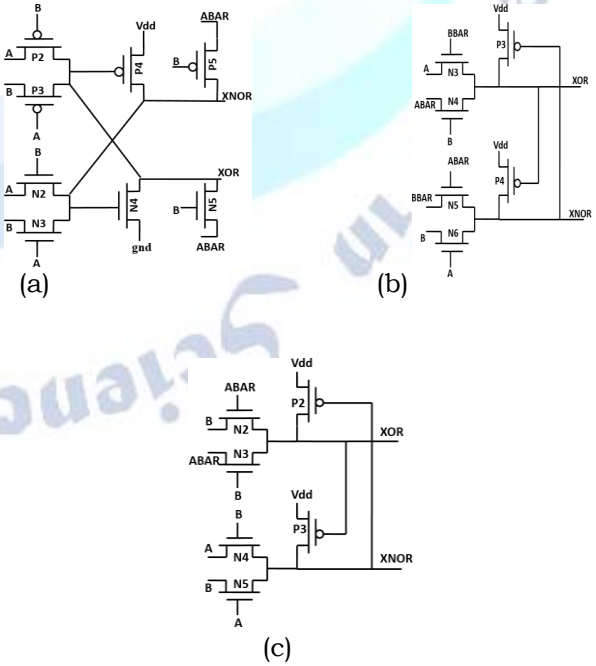


*Fig.3. (a)-(c) Cross Coupling Architecture of XOR/XNOR logic*

The circuit shown in Fig.4 is CPL logic style XOR/XNOR circuit with single inverter. It has two equal charging and discharging paths. First path provides complete swing and second path provides partial swing. The delay as well as power consumption are reduced in XOR/XNOR circuit. It gives the concurrent outputs of XOR/XNOR logic.

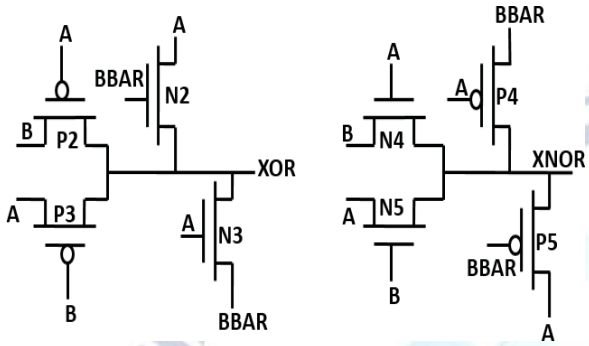


*Fig.4. Modified XOR-XNOR logic generation*

## III. IMPLEMENTATION OF 1-BIT FULL ADDER

A 1-bit Full Adder is designed using XOR-XNOR logic and multiplexer. Two multiplexers are used in this full adder. First multiplexer to generate Sum and the other to generate Carry. A, B are the inputs given to XOR and XNOR circuit and input C is given to selection line of first multiplexer. The outputs Sum and Carry are produced from the multiplexers. The Fig.5 shows the 1-Bit Full Adder circuit.

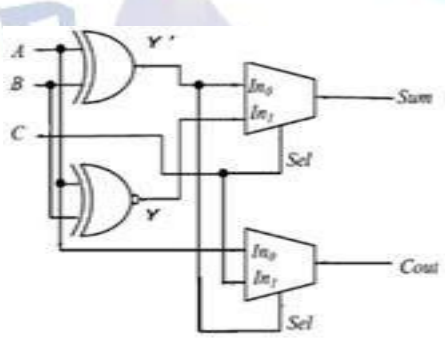


*Fig 5: Implementation of 1-bit Full Adder Circuit*

The Full Adder uses different XOR/XNOR circuits namely Double Pass transistor logic, Pass transistor and Transmission gate logic, Complementary pass transistor logic, Cross coupled architectures and modified XOR/XNOR circuit. All the logics are performed and are used in full adder to get desired output of sum and carry. The full adder circuits are designed in 180nm, 130nm, 90nm, 45nm technologies. It produces complete swing voltage level at output and reduces delay.

## IV. SIMULATION RESULT

The simulation has been donewith different supply voltages to compare the delay as well as power in different technologies. The output waveforms of XOR- XNOR circuit are represented in the Fig.6.

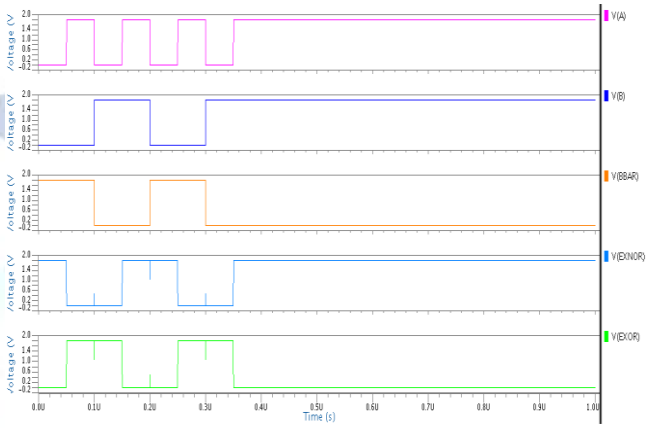


*Fig 6: Output waveforms of XOR-XNOR circuit*

In this different XOR-XNOR logic circuits using different technologies are compared. The Table I represents the comparison table of power as well as delay using 180nm technology. Table II represents in 130nm, Table III represents in 90nm and Table IV in 45nm technologies.

TABLE I

| 180nm | | | |
|---|---|---|---|
| PARAMETERS | DELAY(S) | | POWER CONSUMPTION(W) |
| | XOR | XNOR | |
| DPL | 159.72p | 99.94n | 685.96n |
| PT&TG | 193.07p | 99.95n | 589.91n |
| CPL | 99.88n | 50.15n | 556.37n |
| MODIFIED CPL | 296.70p | 50.02n | 543.11n |
| CCA 1 | 405.59p | 49.98n | 173.85m |
| CCA 2 | 418.74p | 49.95n | 173.85m |
| CCA 3 | 366.81p | 49.97n | 1.363u |
| MODIFIED XOR/XNOR | 9.58p | 50.00n | 731.01n |

TABLE II

| 130nm | | | |
|---|---|---|---|
| PARAMETERS | DELAY(S) | | POWER CONSUMPTION(W) |
| | XOR | XNOR | |
| DPL | 147.44p | 49.93n | 256.20n |
| PT&TG | 164.96p | 49.96n | 194.53n |
| CPL | 50.16n | 50.00n | 261.63n |
| MODIFIED CPL | 242.03p | 50.01n | 310.40n |
| CCA 1 | 261.35p | 49.82n | 920.06n |
| CCA 2 | 299.37p | 49.81n | 958.94n |
| CCA 3 | 217.29p | 49.84n | 173.85m |
| MODIFIED XOR/XNOR | 6.530p | 50.00n | 289.12n |

TABLE III

| 90nm | | | |
|---|---|---|---|
| PARAMETERS | DELAY(S) | | POWER CONSUMPTION(W) |
| | XOR | XNOR | |
| DPL | 147.33p | 49.92n | 136.54n |
| PT&TG | 122.6p | 49.92n | 66.32n |
| CPL | 211.49p | 49.99n | 218.23n |
| MODIFIED CPL | 171.02p | 50.00n | 253.80n |
| CCA 1 | 223.03p | 49.80n | 559.80n |
| CCA 2 | 218.14p | 49.80n | 656.61n |
| CCA 3 | 211.76p | 49.81n | 816.61n |
| MODIFIED XOR/XNOR | 5.269p | 50.00n | 144.76n |

TABLE IV

| 45nm | | | |
|---|---|---|---|
| PARAMETERS | DELAY(S) | | POWER CONSUMPTION(W) |
| | XOR | XNOR | |
| DPL | 134.42p | 49.89n | 53.65n |
| PT&TG | 120.09p | 49.89n | 19.87n |
| CPL | 159.68p | 49.98n | 75.52n |
| MODIFIED CPL | 166.75p | 49.97n | 113.19n |
| CCA 1 | 190.74p | 49.79n | 197.58n |
| CCA 2 | 212.12p | 49.79n | 218.06n |
| CCA 3 | 206.40p | 49.80n | 299.15n |
| MODIFIED XOR/XNOR | 4.77p | 50.00n | 45.86n |

A. Full Adder Results

The output waveforms of 1-bit full adder circuit are represented in figure 7

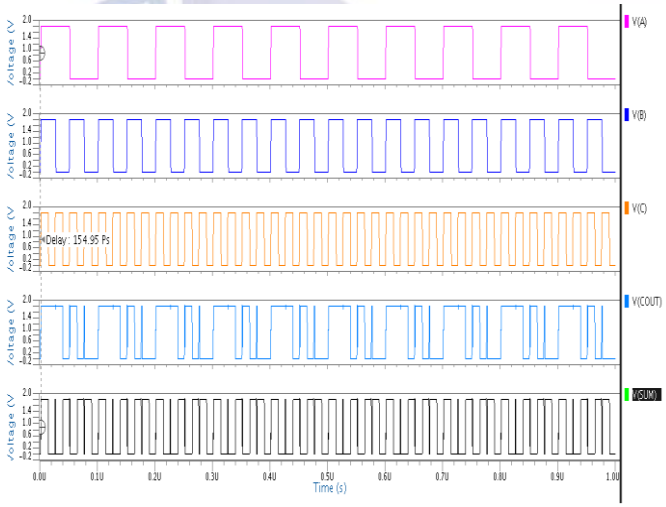


*Figure 7: Output waveforms of 1-bit Full adder*

In this different Full Adders, which are designed using different XOR-XNOR circuits are compared. The Tables represent the comparison tables of power as well as delay using different technologies.

The Table V represents the comparison tableof 180nm technology, Table VI represents 130nm, Table VII represents 90nm, Table VIII represents 45nm technologies.

TABLE V

| 180nm | | |
|---|---|---|
| PARAMETERS | DELAY(S) | POWER CONSUMPTION(W) |
| FULL ADDER 1 | 24.92n | 12.82µ |
| FULL ADDER 2 | 24.85n | 9.78µ |
| FULL ADDER 3 | 24.78n | 9.63µ |
| FULL ADDER 4 | 24.62n | 10.90µ |
| FULL ADDER 5 | 38.23p | 110.65µ |
| FULL ADDER 6 | 36.95p | 110.61µ |
| FULL ADDER 7 | 39.13p | 110.62µ |
| FULL ADDER 8 | 149.33p | 11.66µ |

TABLE VI

| 130nm | | |
|---|---|---|
| PARAMETERS | DELAY(S) | POWER CONSUMPTION(W) |
| FULL ADDER 1 | 105.52p | 9.69µ |
| FULL ADDER 2 | 98.09p | 7.79µ |
| FULL ADDER 3 | 146.16p | 8.53µ |
| FULL ADDER 4 | 146.18p | 9.35µ |
| FULL ADDER 5 | 36.76p | 12.75µ |
| FULL ADDER 6 | 36.95p | 13.25µ |
| FULL ADDER 7 | 38.58p | 15.03µ |
| FULL ADDER 8 | 98.09p | 8.93µ |

TABLE VII

| 90nm | | |
|---|---|---|
| PARAMETERS | DELAY(S) | POWER CONSUMPTION(W) |
| FULL ADDER 1 | 87.69p | 8.711µ |
| FULL ADDER 2 | 70.08p | 2.91µ |
| FULL ADDER 3 | 54.38p | 2.97µ |
| FULL ADDER 4 | 56.74p | 8.10µ |
| FULL ADDER 5 | 35.84p | 9.31µ |
| FULL ADDER 6 | 35.39p | 9.70µ |
| FULL ADDER 7 | 36.71p | 10.57µ |
| FULL ADDER 8 | 70.11p | 7.95µ |

TABLE VIII

| 45nm | | |
|---|---|---|
| **PARAMETERS** | **DELAY(S)** | **POWER CONSUMPTION(W)** |
| **FULL ADDER 1** | 48.70p | 2.94µ |
| **FULL ADDER 2** | 32.33p | 1.07µ |
| **FULL ADDER 3** | 5.55p | 1.08µ |
| **FULL ADDER 4** | 5.61p | 3.22µ |
| **FULL ADDER 5** | 25.48p | 3.21µ |
| **FULL ADDER 6** | 25.10p | 3.25µ |
| **FULL ADDER 7** | 22.89p | 3.57µ |
| **FULL ADDER 8** | 32.30p | 2.71µ |

## V. CONCLUSION

Different logic styleshelp the designer to pick up a suitable design style depending on the requirement. In this modified XOR/XNOR logic is performed using different logic styles. These are used to implement different full adder circuits. The different XOR/XNOR circuits and full adders are designed and compared with delay as well as power consumption using different technologies.

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