Available online at: http://www.ijmtst.com/vol6issue03.html

International Journal for Modern Trends in Science and Technology

ISSN: 2455-3778 :: Volume: 06, Issue No: 03, March 2020

Design and Implementation of Ripple Carry Adder using Various CMOS Full Adder Circuits in 180nm and 130nm Technology

V Haribabu[1] | Ch Malasri[1] | O Jyothirmai[1] | T Pranathi[1]

[1]Department of Electronics and Communication Engineering, Malla Reddy Institute of Technology and Science, Hyderabad, Telangana, India

To Cite this Article

V Haribabu, Ch Malasri, O Jyothirmai, T Pranathi, "Design and Implementation of Ripple Carry Adder using Various CMOS Full Adder Circuits in 180nm and 130nm Technology", *International Journal for Modern Trends in Science and Technology*, Vol. 06, Issue 03, March 2020, pp.:29-33.

Article Info

Received on 05-February-2020, Revised on 16-February-2020, Accepted on 28-February-2020, Published on 03-March-2020.

ABSTRACT

This paper aims of designing of 4-bit ripple carry adder using various CMOS full adder circuits and comparing with various technologies of TSMC library. Full adder is used in various applications like signal processing, arithmetic operations, and multiplexers and so on. This defines the need and importance of designing an adder block in a viable manner. In this Performance is measured for both 180nm and 130nm technologies. For schematic design we are using pyxis schematic produced by mentor graphics. The comparative analysis of different adders is covered here with number of transistors or gate count, delay, average power and power-Delay-product. These are the first concern parameters for measuring of design performance. In ripple carry adder design to achieve best performance metrics various components like inverter, transmission gate, and pass transistors are used.

KEYWORDS: Full adder, high speed, low power, reduced area.

I. INTRODUCTION

The exponential development in versatile and compact gadgets has set out on new difficulties in rapid and low- power Very Large Scale Integration (VLSI) structure. Compactness requires little measure and long-life battery tasks, while the expanding request of advanced preparing speeds need structure of fast microelectronic circuits. In the most recent decade with the coming of advanced cells, practically all sign preparing gadgets are turning into the piece of solitary equipment. From simple calculator to complex image processing, our smart phone contains hundreds of applications which were the part of separate device in the past. The arithmetical operations like addition, subtraction, multiplication, division, numerical integration, convolution, and filtration are performed on a computational unit, the full adder. The complex calculations of today's' versatile applications request support of rapid and low force equipment. As of late, the expansion of microwave frequencies for 5G organizes in the accessible data transfer capacity has radically expanded the reachable information rate. The higher date pace of 5G systems will help incorporate the billion of Internet-of-Thing (IOT) gadgets. All these carrier level nodes and subscriber level devices would require high speed, low power, and small size realization.

The VLSI design engineers are continuously working on these design metrics to satisfy the current and future developments. Addition is the main arithmetic operation. Binary adder is used in many different operations such as addition, subtraction, multiplications, division, and so on. The full adder is a basic unit of binary adder which is a critical component of arithmetic logic unit (ALU) in all types of microprocessors. Since full adder is 1- bit adder to perform n-bit addition ripple carry adder is designed.

A. Ripple Carry adder

Ripple carry adder is a type of combinational logic circuit used in addition of two n-bit binary numbers. 4-bit ripple carry adder is designed for adding two 4-bit binary numbers. Whereas N-bit ripple carry adder is employed for addition of two N-bit binary numbers. Ripple carry adder is a logic circuit in which the carry output of each full adder block is given as the input to the next stage of full adder.

The basic block diagram of 4-bit ripple carry adder is shown in figure.1. It is called as a ripple carry adder because each carry output bit gets rippled into the next stage of the adder . If the carry input of first block is 0 that block acts as half adder then the whole circuit becomes 3-bit full adder with one half adder.

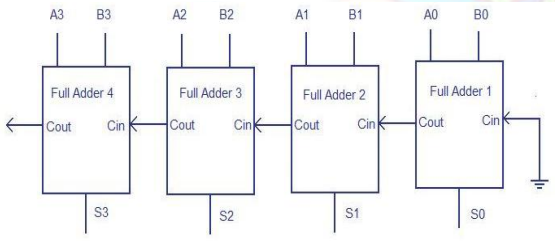


Fig. 1: Ripple Carry Adder

Table 1: Truth table for ripple carry adder

A0	A1	A2	A3	B0	B1	B2	B3	Ci	S0	S1	S2	S3	Co
0	0	0	0	1	1	1	1	0	1	1	1	1	0
0	0	0	0	0	0	0	1	1	1	0	0	1	0
1	0	0	1	0	0	1	0	1	0	1	1	1	0
0	0	1	1	0	0	1	1	1	1	0	0	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

II. FULL ADDERS

A. High Speed 28T Full Adder

The 28- transistor full adder has been presented. Figure 2 represents a full adder designed using DPL logic design style to get the logic of XOR and XNOR and a multiplexer logic using pass transistor to get the S0 output. AND/OR gates are designed to decrease the delay in critical path of carry out signal using a power and ground less pass transistor configuration, respectively. And to get the C0 output from multiplexer a pass transistor is employed. This 28T full adder suffers from increased area due to more number of transistors.

B. CMOS and TG based 16T Full Adder

The sum output of the adder is obtained with XNOR modules. The inverter comprises of PMOS and NMOS transistors which invert the input logic. The average power (34.6 µW) of the circuit was decreased by the incorporation of very weak CMOS inverters coupled with strong transmission gates for 1.8 V supply when implemented at 180-nm technology. For 130-nm technology operated at 1.3-V power supply, average power consumption and delay values are 7.13µW and 10.39ps respectively.

C. Low Power High Speed 15T Full Adder

To decrease the transistors PTL logic is used in full adder design. Low power high speed full adder requires reduced number of transistors in comparison to other full adder techniques. This full adder is found to reduce the delay and give some power saving and time compared to 28T transistor full adder. Hence the power delay product and area also gets reduced.

D. XOR and TG Based Low Power 14T Full Adder

The required number of transistors for the design of this full adder is 14. Half sum is produced by using transmission gate theory and 2nd half of the circuit give the sum and carry outputs. This full adder gives minimal power dissipation because the signal coming to the full adder circuit has a limited path to ground. Because of the path followed from the input to output delay gets reduced.

E. High Speed and Energy Efficient 10T Full Adder

Here we presented a full adder design using as few as ten transistors. This design employs inverter buffered XOR/XNOR logic to improve

driving capability facilities faster operations which leads to less energy consumptions. In spite of the threshold loss problem this full adder can achieve competitive speed performance while using much smaller transistor count. Power consumption is also superior to that of higher transistor count designs. If specific input is applied power dissipation can be further minimized.

F. Low Power 10T Full Adder

10T are required for this design. Because of this average power got reduced in comparison to other designs. This adder has the threshold loss problem. This full adder is used in multiplexers despite of the threshold loss problem. For 180 nm technology this design gives better power consumption compared to all the other designs. Power consumption is moderate and delay will be more for this circuit. In 130 nm technology power consumption and power dissipation are obviously better than the other designs. But the problem is delay will be more for this circuit. So, the conclusion is that we can use this design for Low power applications. But due to high delay in both the technologies this design is not useful for high speed applications.

G. 14T CMOS Full Swing Full Adder

The transistors used for this design are 14. This design uses 6T XNOR/XOR gate to get sum. Here the name full swing means output voltage is identical as the input. From this we can conclude there is no distortion present in this design. In this design we are using transmission gate. The important application of transmission gate is that it overcomes the weak logic problem so output voltage is same as the input. For 180 nm delay, power consumption and power dissipation values are low compared to other designs. In 130nm technology delay and power dissipation values low compared to all the circuits. Power consumption will be moderate. From the evaluation we can conclude that this full adder performs better in all the performance metrics.

H. 14T Hybrid Full Adder

Hybrid full adder means it is the combination of pass transistor circuit and CMOS inverter approach. In this circuit 3 PMOS transistors and 3 NMOS transistors are used to get XOR logic. One 2T multiplexer is used in getting sum and another 2T multiplexer is used as to get carry. In 180 nm technology power consumption, power dissipation and delay values are moderate. In 130 nm technology power dissipation will be low and power consumption and delay values are moderate. The less power dissipation of this full adder is makes it energy efficient.

III. RIPPLE CARRY ADDER DESIGN AND ANALYSIS

Here the main aim is to find out the best design which performs better according to our application. Ripple carry adder is designed by connecting the carry input of each full adder with the succeeding next full adder. Here the ripple carry is designed using various CMOS full adders mentioned above. The design is performed in both 180nm and 130nm technologies. Analysis is done by finding the values of power dissipation, delay and power consumption and comparing in 180nm and 130nm technologies.

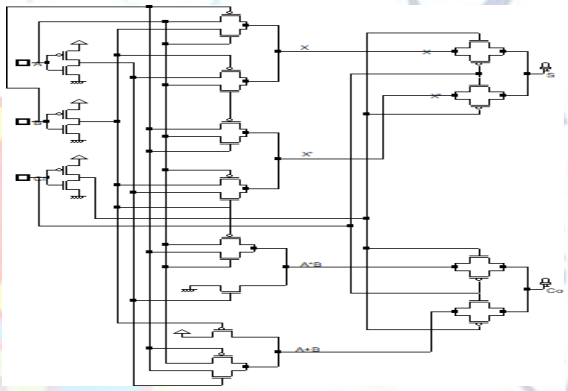


Fig 2: 28T Full Adder

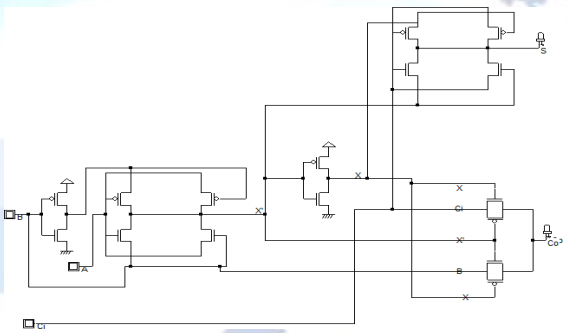


Fig 3: CMOS and TG based 16T Full Adder

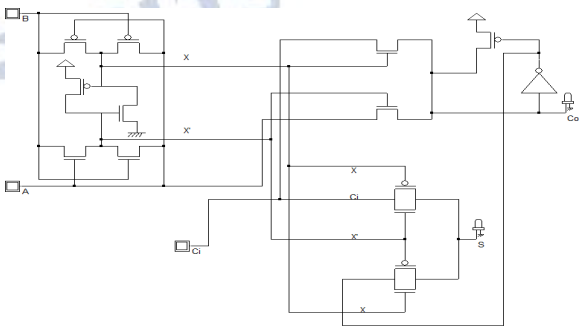


Fig 4: Low Power 15T Full Adder

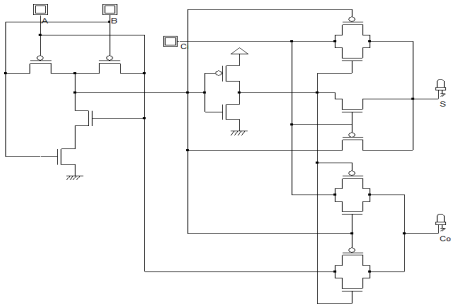


Fig 5: XOR and TG based 14T Full Adder

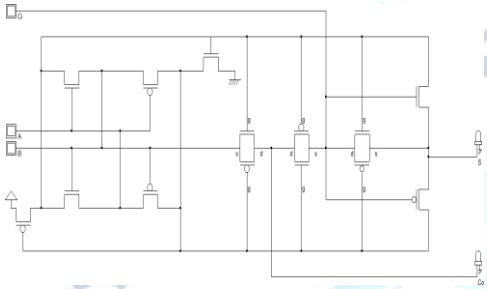


Fig 6: 14T CMOS Full Swing Full Adder

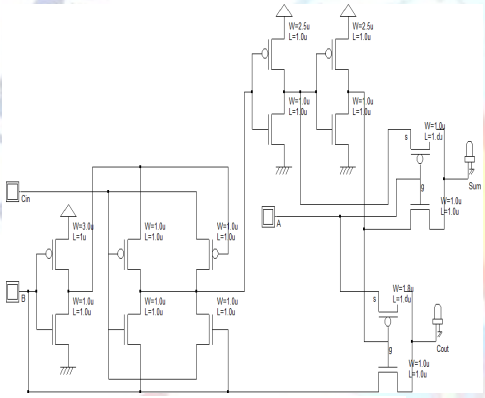


Fig 7: 14T Hybrid Full Adder

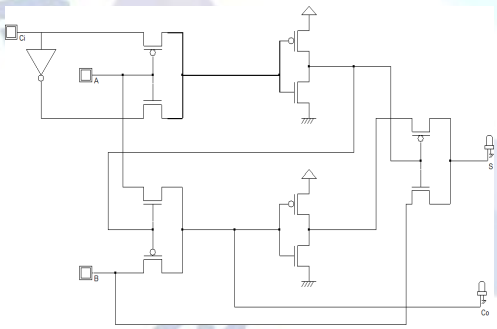


Fig 8: Energy efficient 10T Full Adder

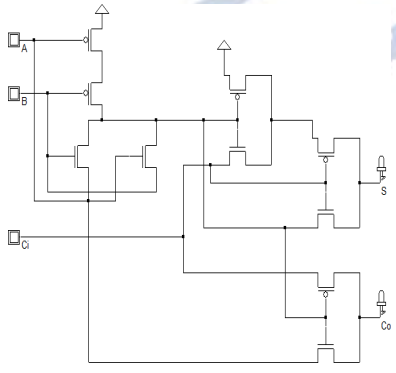


Fig 9: 10T Full adder

IV. SIMULATION RESULTS FOR FULL ADDER

The simulation is performed in mentor graphics tool using pyxis schematic. The circuits are implemented with 130nm and 180nm technologies with supply voltage of 1.3V and 1.8V respectively. Transistor sizes in 180 nm technology for PMOS are W/L=0.36/0.18ns and for NMOS W=L=0.18 and delay is 1ns in both technologies.

A. Analysis in 180nm Technology

From the analysis in case of delay and average 14T CMOS full swing full adder offers higher overall performance.

B. Analysis in 130nm Technology

From the analysis in case of delay 15T full adder gives lower delay and low power 10T full adder gives less power consumption.

V. SIMULATION RESULTS FOR RIPPLE CARRY ADDER

A. Analysis in 180nm Technology

From the analysis in180nm technology in case of delay XOR and transmission gate based 10T ripple carry adder performs better. In case of average power 15T full adder performance is better. From the overall analysis 10T ripple carry adder performs better compared to all other circuits.

B. Analysis in 130nm Technology

From the analysis in 130nm technology in case of delay CMOS and transmission gate based adder gives lower delay and in case of power consumption 15T adder gives lower power consumption.

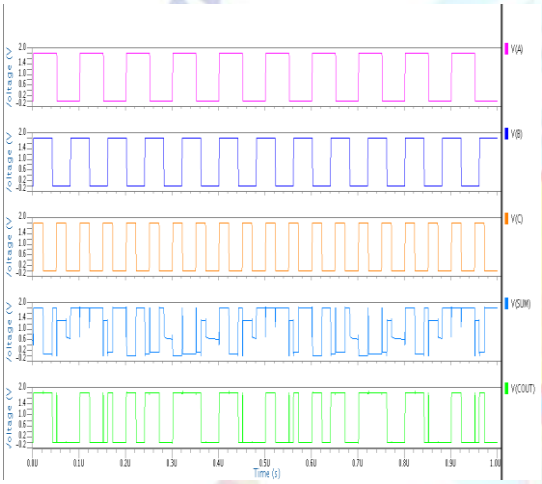
C. Comparison Table for Full Adder

Full Adder	Delay		Average power	
	180	130	180	130
Fig[2]	41.13ns	1ns	57.13µw	168.85µw
Fig[3]	17.24ps	34.44ps	1.13µw	166.42µw
Fig[4]	7.14ps	10.4ps	34.69µw	7.13µw
Fig[5]	41.25ns	136.83ps	39.75µw	84.36µw
Fig[6]	2.87ps	11.31ps	1.66µw	5.13µw
Fig[7]	51.13ns	48.82ns	9.94µw	12.33µw
Fig[8]	42.10ns	38.01ps	14.50µw	17.65µw
Fig[9]	61.11ns	41.17ns	3.33µw	2.00µw

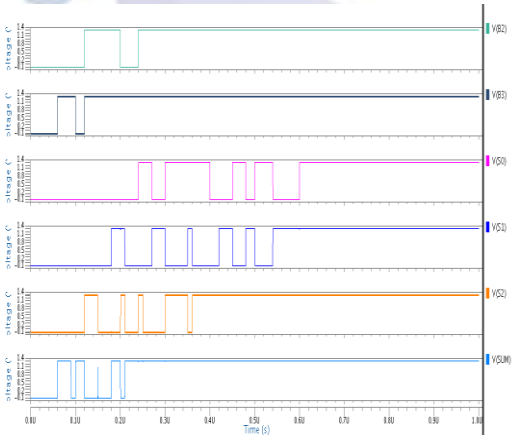
D. Compression Table for Ripple Carry Adder

Ripple Carry Adder	Delay		Average power	
	180	130	180	130
Fig[2]	60.09ns	60.11ns	3.70µw	403.43µw
Fig[3]	10.22ns	47.84ps	641.64nw	201.46µw
Fig[4]	135.22ps	240.49ps	19.98µw	3.70µw
Fig[5]	84.02ps	91.09ps	53.58µw	108.26µw
Fig[6]	97.75ps	30.01ns	985.62nw	6.27µw
Fig[7]	91.15ns	60.45ns	15.55µw	19.03µw
Fig[8]	50.64ns	60.00ns	5.84µw	13.81µw
Fig[9]	90.44ns	52.55ps	2.8µw	4.38µw

E. Full adder waveform



F. Ripple carry adder



VI. CONCLUSION

In this paper, we have implemented ripple carry adder using various full adders. We have estimated the values of power, delay for various full adder and compared the values in 180nm and 130nm technologies using mentor graphics tool from the analysis we can say that no single design can give Performance factors as good as we required. So, the selection of the design depends on the application needs.

REFERENCES

[1] N. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed. USA: Addison-Wesley Publishing Company, 2010.

[2] J.-F. Lin, Y.-T. Hwang, M.-H. Sheu, and C.-C. Ho, "A Novel High-Speed and Energy Efficient 10-Transistor Full Adder Design," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 54, no. 5pp. 1050–1059, May 2007

[3] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits: A design Perspective, 3rd ed. Pearson Education, 2006, 00000.

[4] M. Aguirre-Hernandez and M. Linares-Aranda, "CMOS Full-Adders for Energy-Efficient Arithmetic Applications," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 4, pp. 718–721, Apr. 2011.

[5] C.-K. Tung, S.-H. Shieh, and C.-H. Cheng, "Low-power high-speed full adder for portable electronic applications," Electronics Letters, vol. 49 no. 17, pp. 1063–1064, Aug. 2013.

[6] N. H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design: A Systems Perspective. Boston, MA, USA: Addison-Wesley Longman Publishing Co., Inc., 1985.

[7] N. Zhuang and H. Wu, "A new design of the CMOS full adder," IEEE journal of solid-state circuits,vol. 27, no. 5, pp. 840–844, 1992. [Online]. Available:ftp://220.135.93.233/My Book/JSSC ISSCC database/JSSC ISSCCVLSI19662002/jpdfs/ieee/ssc/jssc/1992027/05may/0840zhua.pf

[8] P. Bhattacharyya, B. Kundu, S. Ghosh, V. Kumar, and A. Dandapat,"Performance Analysis of a Low-Power High-Speed Hybrid 1-bit FullAdder Circuit," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. PP, no. 99, pp. 1–8, 2014.