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# All-optical Frequency Divider using TOAD based D-Flip-Flop

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## ABSTRACT

*From the last few decades the optical communication has been established as much easier process than electrical communication. Many optical proposed circuits have already been suggested in many fields in support of this. The optical communication circuits demand frequency dividers capable of operating well above 10 GHz. Here, an all-optical frequency divider using terahertz optical asymmetric demultiplexer (TOAD) based D-flip-flop is proposed in the optical domain in a configuration exactly like the standard electronic setup. It presents a high-speed flip-flop-based frequency divider incorporating a new high-speed latch topology with satisfactory performance. The proposed all-optical frequency division scheme has been theoretically demonstrated in this paper. In this scheme the input and output binary digits are expressed as the presence (1) and the absence (0) of the light pulses. The performance of this proposed optical realization is evaluated by numerical simulation that confirms its feasibility in terms of the choice of the critical parameters.*

***KEYWORDS:*** *Terahertz Optical Asymmetric Demultiplexer (TOAD), R-S and D-flip-flop, Frequency Divider.*

## I. INTRODUCTION

To overcome the electronic bottlenecks, here the advantages of optical fiber communication are exploited fully without need of optical-electrical-optical (OEO) conversions. [1-3]. TOAD and semiconductor optical amplifier (SOA)-assisted gates effectively combine fast switching time and benefits of reasonable noise figure [4-10]. The all-optical frequency divider using TOAD based D flip-flop is designed in a configuration exactly like the standard electronic setup. More specifically, this realization would develop ultrahigh speed diagnostic and measurement equipment with comparative performance over their electronic counterparts. The goal of this work is to propose frequency division in all optical domains in an affordable, controllable and realistic manner. Simulation results support the above claims.

## STRUCTURE OF PAPER

This paper is organized as follows: Section II describes briefly the basic operation of TOAD based optical system. Section III presents optical realization of binary D flip-flop using binary S-R flip-flop. Section IV explains all-optical frequency divider using TOAD based D flip-flop in the optical domain. Section V presents simulation results. Finally, the concluding remarks are made in Section VI.

**OBJECTIVES**

The objective of this research work is to propose frequency divider in all optical domains in an affordable, controllable and realistic manner. The simulation results confirm the above design.

## II. OPERATION PRINCIPLE OF TOAD-BASED OPTICAL SWITCH

The SOA-based TOAD switches are important by their characters of fast switching time, low power consumption, high repetition rate, low latency, noise and tolerance, compactness, high nonlinear properties and thermal stability. These all properties enable their efficient exploitation in a real ultra-high speed optical communications environment [16]. From the last century, TOAD based gate has taken an important role in optical communication and information processing [4-16]. The SOA-based TOAD switches can perform demultiplexing at Tb/s [19-20]. The TOAD consists of a loop mirror with an additional intraloop 2×2 (ideally 50:50) coupler. The loop contains a control pulse (CP) and a nonlinear element (NLE) that is offset from the loop's midpoint by a distance Δx as shown in Fig. 1(a).

The electrical field at port-1 and port-2 can be expressed as follows:

$$\underline{E}_{out,1}(t) = \underline{E}_{in}(t-t_d)\cdot e^{-j\omega t_d}\cdot\left[d^2\cdot \underline{g}_{cw}(t-t_d) - k^2\cdot \underline{g}_{ccw}(t-t_d)\right] \quad \ldots (1)$$

$$\underline{E}_{out,2}(t) = jdk\underline{E}_{in}(t-t_d)\cdot e^{-j\omega t_d}\cdot\left[\underline{g}_{cw}(t-t_d) + \underline{g}_{ccw}(t-t_d)\right] \ldots (2)$$

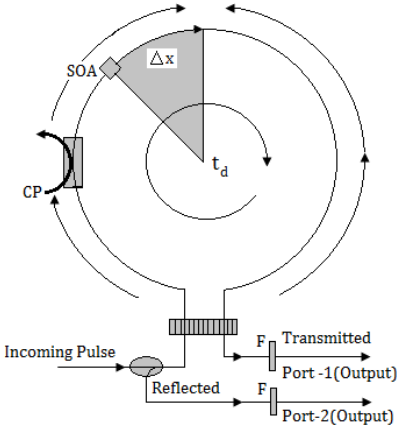
Where, $t_d$ is pulse round trip time within the loop as shown in the Fig. 1. Coupling ratios $k$ and $d$ indicate the cross and through coupling, respectively. The cw signal is amplified by the complex field gain, $\underline{g}_{cw}(t)$, while ccw by $\underline{g}_{ccw}(t)$. The output power at port-1 can be expressed as, while ccw by $\underline{g}_{ccw}(t)$. The output power at port-1 can be expressed as,

$$P_{out,1}(t) = \frac{P_{in}(t-t_d)}{4}\cdot\left\{G_{cw}(t)+G_{ccw}(t)-2\sqrt{G_{cw}(t)\cdot G_{ccw}(t)}\cdot\cos(\Delta\varphi)\right\}$$

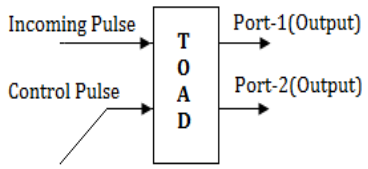
$$= \frac{P_{in}(t-t_d)}{4}\cdot SW(t) \quad \ldots (3)$$

Here, $SW(t)$ is the transfer function. The phase difference between cw and ccw pulse is defined by $\Delta\varphi = (\varphi_{cw} - \varphi_{ccw})$ .The symbols $G_{cw}(t), G_{ccw}(t)$ indicate the respective power gains. Power gain is related with the field gain as $G = g^2$ and $\Delta\varphi = -\frac{\alpha}{2}\cdot\ln\left(\frac{G_{cw}}{G_{ccw}}\right)$. Now we will calculate the power at port-2 $P_{out,2}(t) = \frac{1}{2}\underline{E}_{out,2}(t)\cdot\underline{E}^*_{out,2}(t)$

$= d^2k^2\cdot P_{in}(t-t_d)\cdot\left\{G_{cw}+G_{ccw}+2\cdot\sqrt{G_{ccw}\cdot G_{cw}}\cdot\cos[\Delta\varphi]\right\}$ … (4)




(a)




(b)

Fig: 1(a) TOAD based optical switch, 1(b) Schematic diagram of 1(a)

Table-I: Truth Table of TOAD

| Incoming Pulse | Control Pulse | Port-1 | Port-2 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

For an ideal 50:50 coupler, d 2=k 2=1/ 2. In the absence of the control pulse (CP), the data signal (Incoming pulse, IP) enters the fiber loop. While the cw and ccw pulses pass through the SOA at different times, they experience the same unsaturated amplifier gain (Gcw = Gccw = Go) before recombining at the input coupler. In other words, Δ ϕ=0, resulting in Po, 1=0 and Po, 2=Go Pi. When a control pulse is injected into the loop it saturates the SOA changing its index of refraction resulting in the counter-propagating pulses

experiencing different gain saturation profiles, resulting in a non-zero output on port-1. (Note that in this analysis the presence of a light pulse is '1' and the absence is interpreted as '0') The resulting truth table is shown in Table 1. As can be seen in Table 1, the output of port-1 corresponds to a logical IP AND CP and the output of port-2 corresponds to IP AND NOT CP operation.

## III. BINARY D FLIP-FLOP USING BINARY S-R FLIP-FLOP

An S-R flip-flop has two inputs (S and R) and two outputs Qn+1 and $\overline{Q}$n+1. The three conditions of this flip-flop are "Hold" (S=R=0), "Reset" (S=0, R=1) and "Set" (S=1, R=0) [9]. Using TOAD we have designed an all-optical 1-bit binary memory unit (latch), which is shown in Fig. 2(a). In this circuit, the TOAD is used like a binary NOT gate. 'S' and 'R' are the two binary inputs and are connected to switches $S_1$ and $S_2$ through wavelength converter (WC) that change the wavelength of the light pulse and erbium doped fiber amplifier (EDFA) to increase the optical power of the control signal. In our configuration a constant pulse light source (CPLS) is used to provide the incoming signals to the two TOADs ($S_1$ & $S_2$). The signals coming out through the reflected ports, which correspond to port 2 in Fig 1 (b) give the flip-flop outputs Qn+1 and $\overline{Q}$n+1. A part of the output Qn+1 and $\overline{Q}$n+1 are fed back to S and R inputs, respectively, with the help of a beam splitter (BS) and a beam combiner (BC). Here the presence of light is taken as '1' state and the absence of light is taken as '0' state. Therefore the outputs for different inputs combinations are as follows: Case 1: When S=0 and R=1, according to the TOAD principle of operation $S_{2L}$ receives no light, i.e. Qn+1 =0. As it is connected to input 'S', then $CP_1$=0 and so $S_{1L}$ receives light, which means that $\overline{Q}$n+1 =1. Now Qn+1 and $\overline{Q}$n+1 are connected to the S and R inputs, respectively. If both the signals are withdrawn, i.e. S=R=0, then Qn+1 and $\overline{Q}$n+1 retain the same value. Case 2: When S=1 and R=0, like the previous explanation we obtain Qn+1=1 and $\overline{Q}$n+1 =0, which is locked even if we assign R=S=0. Case 3: When S=R=1, both S1 and S2 switches receive the incoming and control signal, so the lower outputs of both the TOADs receive no light, i.e. $\overline{Q}$n+1 = $\overline{Q}$n+1 =0. The stored data is cleared from memory and this state is "forbidden". Binary D flip-flop can be constructed by S-R latch and a binary NOT gate. Implementation in all-optical form may be realized by a TOAD ($S_3$), as shown in Fig. 2(b), in such a way that the "forbidden" state (S=R=1) never happens. Here light from the input D is split by a BS and connected to the $S_3$ through WC and EDFA. This may act as control signal. The incoming signal of switch S3 is taken from a CLS. If input D receives a light pulse, $C_1$ receives no light (as both the incoming and control signals of S3 are present, hence light passes through the upper channel of S3). If D=0, $C_1$ receives light (as the control signal of $S_3$ is absent). Here input D is connected to S and $C_1$ is connected to the 'R' input of the S-R flip-flop unit.

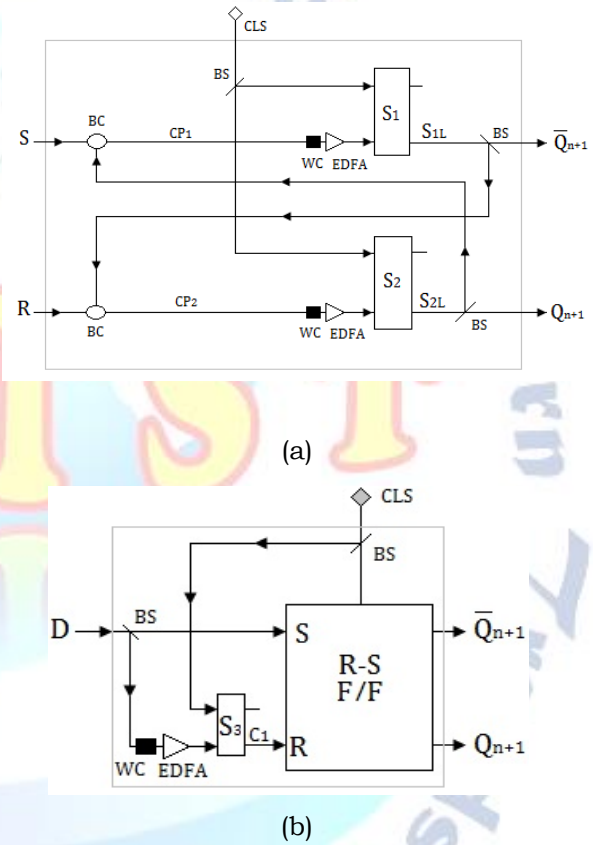



Fig: 2(a) All-optical binary S-R flip-flop, (b) All-optical D flip-flop

## IV. D-FLIP-FLOP FOR FREQUENCY DIVISION

One main use of a D-type flip flop is as a Frequency Divider as shown in Fig. 3. If the Q output on a D-type flip-flop is connected directly to the D input giving the device closed loop "feedback", successive clock pulses will make the bistable "toggle" once every two clock cycles. The Data Latch can be used as a "Binary Divider", or a "Frequency Divider" to produce a "divide-by-2" counter circuit, that is, the output has half the frequency of the clock pulses. By placing a feedback loop around the D-type flip flop another

type of flip-flop circuit can be constructed called a T-type flip-flop or more commonly a T-type bistable that can be used as a divide-by-two circuit in binary counters as shown below.

It can be seen from the frequency waveforms above, that by "feeding back" the output from Q to the input terminal D, the output pulses at Q have a frequency that are exactly one half ( $f/2$ ) that of the input clock frequency, ( $f_{\text{in}}$ ). In other words the circuit produces frequency division as it now divides the input frequency by a factor of two (an octave) as Q = 1 once every two clock cycles.

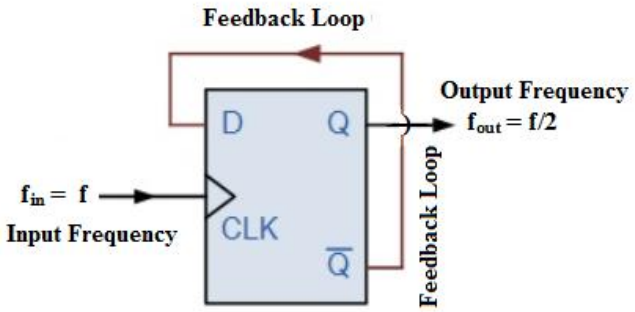



Fig. 3 D-flip-flop based Frequency Divider

The templating system has plugins available to match line items and tables in an invoice. Using YAML templating allows flexibility for users to quickly add new invoice templates to the system by quickly creating a template for it and the system can process invoices based on the new templates immediately. This templating system results searches for regex in the raw text and helps return accurate results from an invoice.

## V. SMULATION

Incoming and control pulse energy of every TOAD are Gaussian $\left[\frac{E_0}{\sigma\sqrt{\pi}}\exp\left\{-\left(\frac{t}{\sigma}\right)^2\right\}\right]$ in nature. The insertion loss (I.L.) of this circuit can be calculated by the following equation:

$$\text{I.L.(dB)} = 10\log\left(\frac{P_{out}}{P_{in}}\right) \quad \ldots (5)$$

The extinction ratio of the TOAD based switch can be calculated by the following equation [17]:

$$Ex.R(dB)\Big|^{OFF} = 10\ log\left(\frac{P_{out,2}}{P_{out,1}}\right)\Bigg|_{Control=off}$$

$$Ex.R(dB)\Big|^{ON} = 10\ log\left(\frac{P_{out,1}}{P_{out,2}}\right)\Bigg|_{Control=on}$$

…(6)

With these formulae we obtain $Ex.R(dB)\Big|^{OFF}$ = very high (because we get $P_{out,1}$ by theory is zero) and $Ex.R(dB)\Big|^{ON} \approx$13 dB. The minimum peak power when the pulse of the payload is high (1) say ( $P^1_{Min}$ ) and the maximum when the pulse is low (0) say ( $P^0_{Max}$ ) [18].

Then, $C.R.(dB) = 10\ \log\left(\frac{P^1_{Min}}{P^0_{Max}}\right)$ … (7)

For all-optical computing and information processing this theoretical model and the results obtained numerically will be useful in future. The simulation is done by setting first the critical parameters are given Table II.

Table-II: Parameters for Simulation

| Parameters | Symbol | Value |
|---|---|---|
| Injection current of SOA | I | 120 mA |
| Unsaturated single-pass amplifier gain | $G_0$ | 17.5 dB |
| Line-width enhancement factor of SOA | $\alpha$ | 7.1 |
| Gain recovery time | $\tau_e$ | 270 ps |
| Saturation energy of the SOA | $E_{sat}$ | 1215 fJ |
| Eccentricity of the loop of TOAD | | 95 ps |
| Control pulse energy | $E_{cp}$ | ~200fJ |
| Full width at half maximum of control pulse | $\sigma$ | 2.05 ps |
| Incoming pulse energy | $E_{in}$ | ~20fJ |

Here, the presence of light is taken as '1'state and absence of light is taken as '0'state. Simulation [16] is done using Matlab-9. The vertical axis in Fig 4 (a) and (b) indicates power in dBm, while horizontal axis represents time scale in ps. The

insertion losses of S-R flip-flop circuit for different inputs are shown in Table III.

Table-III: Insertion loss of S-R flip-flop circuit for different inputs

| S-R flip-flop inputs | | S-R flip-flop outputs(in dB) | |
|---|---|---|---|
| S | R | $Q_{n+1}$ | $\bar{Q}_{n+1}$ |
| 0 | 1 | 11.6 | 6.42 |
| 0 | 0 | 11.6 | 6.42 |
| 1 | 1 | 11.6 | 11.6 |
| 1 | 0 | 6.42 | 11.6 |
| 0 | 0 | 6.42 | 11.6 |
| 1 | 1 | 11.6 | 11.6 |

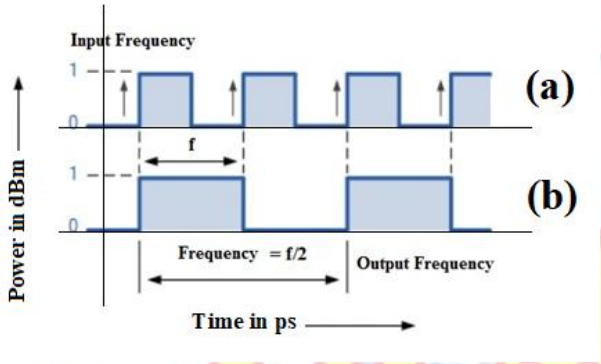



Fig. 4 Output of Frequency Divider

## VI. FUTURE SCOPE AND CONCLUSION

In conclusion, the design of an all-optical frequency divider using TOAD based D-flip-flop has been theoretically addressed and demonstrated. The core building block for these modules is the TOAD. The technical requirements for the critical parameters extracted from the simulation results indicate that the circuit can be implemented with a more than adequate contrast ratio and in a practically feasible way. This verifies that frequency divider can be produced in the optical domain in a straightforward manner, just like its electronic counterpart, without complex modifications in its standard structural form. Intensity losses due to couplers in interconnecting stage may not create much trouble in producing the desired optical bits at the output as the whole system is digital one and the output depends only on the presence or absence of light. The circuit realization is very promising regarding the issues of versatility, re-configurability and compactness. The design can be used and extended for diverse applications for which it is required.

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