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Development of Reduced Switch Multilevel Inverter for Grid Connected Applications

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ABSTRACT

The main focus of this paper is to develop a integrated photovoltaic system with lesser switch count multilevel inverter to feed 300W ac load with better power quality and better efficiency. Multilevel inverters are becoming important in industry because of their highpower capability and low harmonic content. Multilevel inverter has a specialized character for developing separate dc sources. The complexity of switching and gate drive circuits compromise at Objective of this paper is to compare the existing topologies by designing a 7-level modified reduced switch symmetrical MLI (MRSMLI) with seven switches and same voltage sources in each level. Simulation of seven-level seven- switch MLI will be done using MATLAB/SIMULINK environment andA new balanced MLI structure using split voltage sources and a relatively small number of semiconductor switches compare to the existing MLI topologies has been developed.

KEYWORDS: *Conventional multilevel inverter, Diodes, DC Sources, MOSFET's, H bridge inverters, Switches,IGBT*

1. INTRODUCTION

Since 1975, the origin regarding the multilevel inverter technology was first implement. This technology uses more number of dynamic semiconductor devices to perform the voltage alteration in small steps [5]. Compare with conventional power conversion approach, the new topology has numerous advantages. The voltage (dv/dt) stress on the load demand is reduced due to generation of high quality waveforms in small staircase voltage steps and also very much concerned about the electromagnetic compatibility [2]. In this fast modern world the use of high power for factories and industrial application are in high demand and for some medium or low power is needed for its operation. The high power and medium voltage situations are mostly used in the fields of electric motors [12] that require high power source in industrial loads. The alternate to all this problems is been solved by a device called Multilevel

Inverter (MLI). In recent years many literatures has been proposed onmodification to the existing predictable cascaded MLI. The related gate drive circuits are required by every semiconductor switches creates more complexity in mechanical design of inverter. Isolated voltage [8] sources orbank of capacitors produces the small voltage steps in multilevel inverters. One more multilevel inverter may be required for the voltage balancing problem. Latest studyintroduces the new topology of multilevel inverter with specific modulation technique. But most widely used multilevel inverters are cascaded inverter, flying capacitor inverter and neutral-point clamped inverter (NPC). Thereis some novel methods recently recommended[1], where low switching frequency and high power devices are used. The minor change is required to decrease the output voltage distortion, with the drawback of substantial quantity of low order current harmonics.

The precise magnitude of output voltage cannot be obtained because of the utilization of adopted PWM[13]technique. The four level inverter topology which is valid for only even number[9] of steps and also cannot produce the zero state voltage level is proposed. Current technical advancement develops theadditional method, which uses either the fewer amounts of semiconductor switches or the fewer amounts of dc voltage sources according to the requirements. But predictable inverter technology still requires more switches[4] than theproposed topology. The power switches and diodes of different ratings are required, which is most key negative aspect of this topology.

The usages of dc voltage in the proposed topology are of equal value. So, this topology is called as balanced topology. But asymmetrical topology requires different rating voltage sources. According to the configuration the dc voltages are set in accordance with exacting relation between them. In symmetrical topology, this different rating problem also occurs. But a few of high frequency switches can resist maximum overall voltages[10], which limit their exploitation for high-voltage devices only. Another novel method has been proposed, which introduces transformer by replacing some of dc power sources. But the major drawback of this method is addition of so many transformers which enlarges the motorized design and increases the overall inverter cost. Additional number of switches are required than proposed configuration in another method[15]. Capacitor balancing is explained as main disadvantages in so many literatures. A specific optimization technique is used to control theswitching angle of semiconductor switches[14](IGBT) of cascaded H-bridge multilevel inverter. The genetic algorithm (GA) is used for selected harmonic elimination and also to lessenthe total harmonic distortion (THD) of output voltage.

A novel symmetrical multilevel inverter arrangement withless number of components[12], fewer carrier signals and gatedriver circuit is proposed. It is having multilevel DC linkwhich synthesize staircase type dc voltage utilizing a sourceconcoction module and the output waveform is obtain byconventional H-bridge.

Predictable topology uses twelve switches for aseven-level MLI design, whereas recent advancement hasbeen presented with reduced number of switches[8]. I.e. withnine switches, seven switch and six switch. Multilevel Invertersare in a very high demand since a last few years due to theirhigh voltage and medium voltage applications in renewable energy resources. They can withstand high voltage,higher voltage/current harmonics, higher switching losses,high EMI as well as low power quality. There are threedifferent topologies of MLI's like cascaded MLI's, diodeclampedMLI's & flying-capacitor MLI's[7-11]. They have awide range of applications. H-bridge inverters were initiallyintroduced which was later replaced by a series of capacitorbanks while the use of floating capacitors is to clamp theoutput voltage. The main use of H-bridge inverters is todivide the DC-input sources from the DC-output without theuse of a diode or a flying-capacitor. Here we havediscussed about the improvement, enlargement, and the meritsof a CMLI over other MLI topologies. An increase inlevels means more number of switches for its operation. So themain intention now lies how to make simpler the compositecircuit[Fig 4]. Then arises the conception of "switch reduction" thatis to reduce the switches from 12 to 9 and so on basing onexisting topology.

To obtain the necessary ac voltages produced fromthe multilevel inverters, many dc sources are been connectedwhich are obtained from the fuel cells, batteries etc. Thenumber of dc sources is directly proportional to the outputwaveform level. So as the no of dc sources increase, theoutput waveform level also gets increased. The optimistic side ofusing multilevel

inverter[9] includes lower semi-conductorvoltage stress, better harmonic performance, low ElectroMagnetic nosiness (EMI) and lower switchinglosses.

2. PROPOSED MULTILEVEL INVERTER

According to various literatures, it concludes thatmore number of semiconductor switches is required for morenumber of voltage steps. So, the term unfussiness has nomeaning in case of cascaded multilevel inverter. Thesimplification of the complex circuit[2] can be solved by usingReductionsemiconductor technology. The reduction ofswitches of existing seven-level multilevel inverter is carriedout by number of experiment[11]. It gradually decreases from 12to 6 numbers of switches.

A. Seven Level Nine switch MLI

The three dc sources and HBridgewhich comprises of four to extra fiveswitches was shown in Fig1 for producing stepped 7 levels [5] in positive andnegative cycles correspondingly.

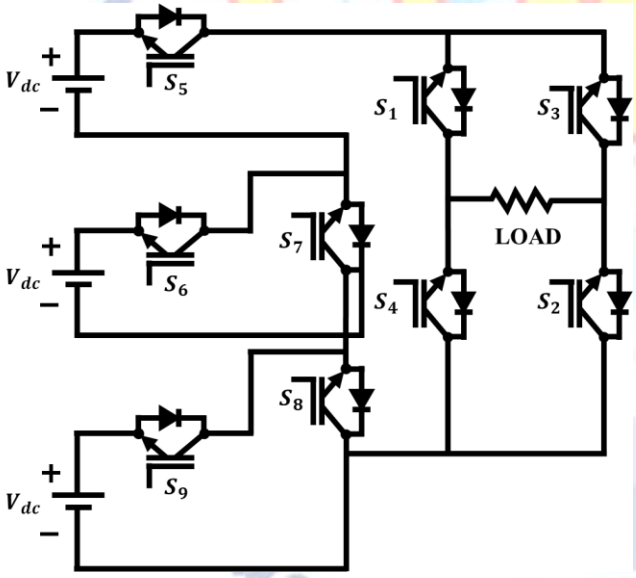

Fig 1. Seven Level Nine Switch Multilevel Inverter

H-bridge inverters were originally introduced which was far along replaced by a series of capacitor banks while the use of floating capacitors is to clamp the output voltage. The number of dc sources is directly proportional to the output waveform level.The power switches and diodes of different ratings are compulsory, which is most key negative aspect of this topology. Totally Nine switches are use in the Multilevel Inverter.

Table 1. Switching Table of seven- level nine-switch MLI

S.NO	S1	S2	S3	S4	S5	S6	S7	S8	OUTPUT VOLTAGE
1.	1	1	1	0	1	0	1	0	+VDC
2.	1	1	0	0	1	1	0	0	+2VDC
3.	1	1	0	0	1	1	0	1	+3VDC
4.	0	0	0	0	0	1	0	0	0
5.	0	0	1	1	0	0	1	0	-VDC
6.	0	0	1	1	0	0	1	1	-2VDC
7.	0	0	1	1	0	0	1	0	-3VDC

1=ON state 0=OFF state

B. Seven Level seven switch MLI

From the Fig2,three dc sources,7 switches and a H bridge for the polarity change. Here, at a time three switches conduct for level generation.

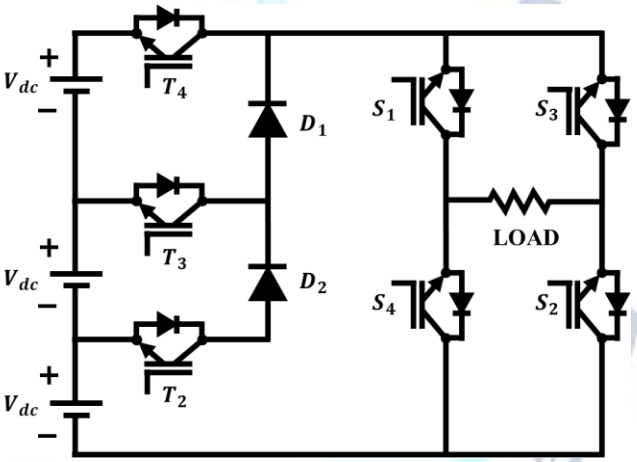

Fig 2. Seven Level Seven Switch Multilevel Inverter

We can observe that the switching devices for the planned inverter at the time of conduction are three. So switching loss[14] is greatly reduces. For each level output only three switches and maximum two diodes conduct.

- It has 7 output voltage levels that is 3V, 2V, V, 0, -V, -2V, -3V
- For attaining the V0 3V, the switches S1, S2, S3 &S4 must be turned on (where V0=output voltage)
- For attaining the V0 2V, the switches S1, S3& S4Must be turned on.
- Similarly for V0 V, switches S3 & S4 must be turned on.
- For 0 all switches should be in off state.
- For –V switches S5 & S6 must be turned on.
- For –2V switches S1, S5 & S6 must be turned on.
- For –3V switches S1, S2, S5 & S6 must be turnedon.

Table 2. Switching Table of seven- level seven-switch MLI

S.NO	S1	S2	S3	S4	T4	T3	T2	OUTPUT VOLTAGE
1.	1	1	0	0	1	0	0	+VDC
2.	1	1	0	0	0	1	0	+2VDC
3.	1	1	0	0	0	0	1	+3VDC
4.	0	0	0	0	0	0	0	0
5.	0	0	1	1	1	0	0	-VDC
6.	0	0	1	1	0	1	0	-2VDC
7.	0	0	1	1	0	0	1	-3VDC

3. SEVEN LEVEL INVERTER WAVEFORM

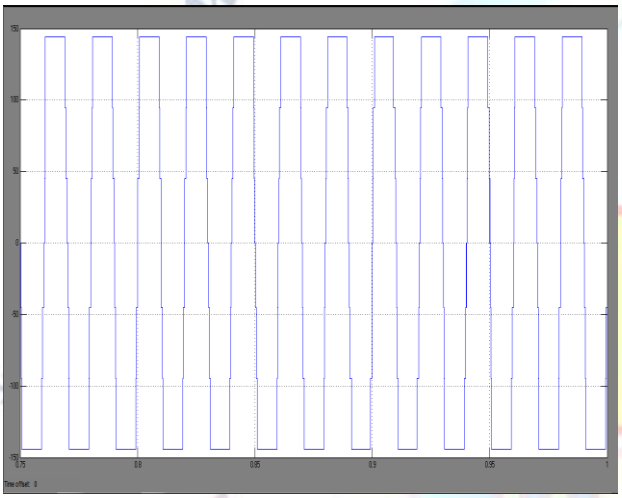

Fig 3.Output Waveform of a 7-level MLI

The simulation of a 7-level seven switch MLI output waveform and It consists the seven levels of 3V, 2V, V, 0, -V, -2V, -3V then the voltage level also same as Nine switch MLI shown in Fig 3.

4. MULTILEVEL INVERTER

Fig 4.Image for MLI

5. SIMULATION RESULTS

A. Simulation of Seven level nine switch MLI

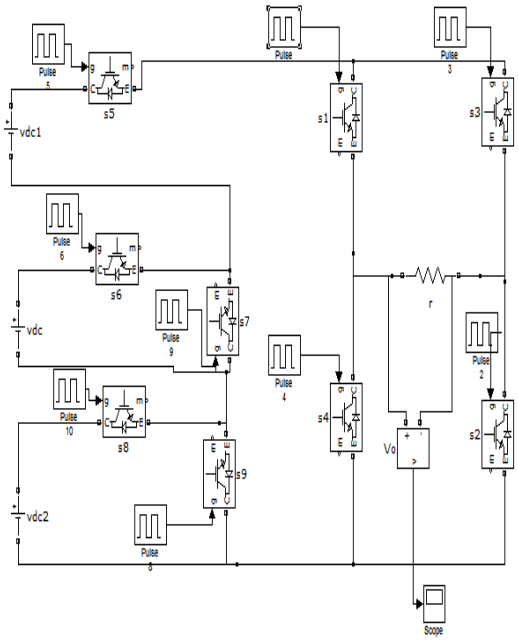

Fig 5. Simulation of Seven Level Nine Switch MLI

Simulation of H-bridge Multilevel Inverter was shown in Fig 5.It of 4 switchesalong with 3 dc sources and 5 more switches for its function and to obtain stepped 7 levels in positive and negative cycle.The power switches and diodes of different ratings are required, which is most key harmful aspect of this topology.

B. Output waveform of seven level nine switch MLI

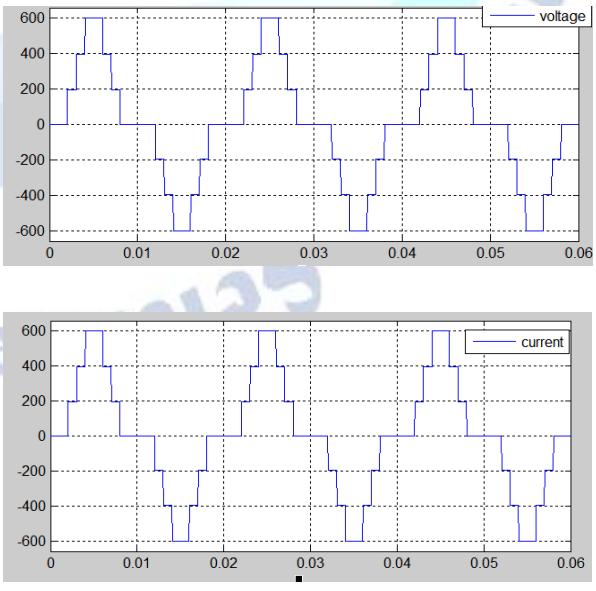

Fig 6.Waveform for Seven Level Nine Switch MLI

Voltage waveform for Multilevel inverter shows in Fig 6.Then the figure give the output waveform of seven level nine switch Multilevel Inverter. The pulse generator value and Phase angle value is varied and also varied the output waveform.

C. Simulation of Seven level seven switch MLI

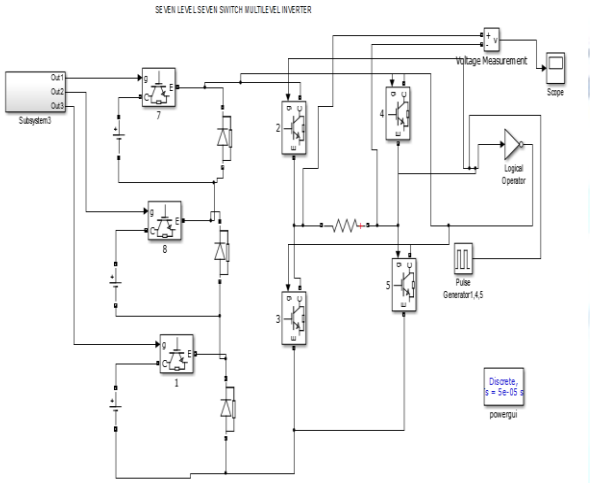

Fig 7. Simulation of Seven Level Seven Switch MLI

The MLI that contains three dc sources in which two dc sources consists of 50V each.Scope ,powergui and load also contain in the Multilevel Inverter. The simulation of a 7-level seven switch Multilevel Inverter was shown in Fig 7.

D. Output waveform of seven level seven switch MLI

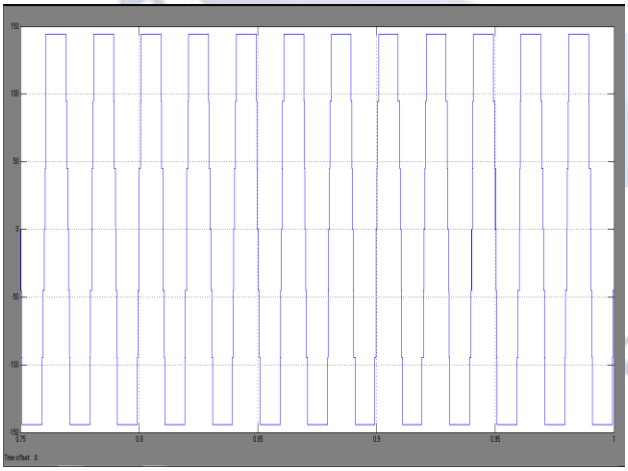

Fig 8.Waveform for Seven Level Seven Switch MLI

It consists the seven levels of 3V, 2V, V, 0, -V, -2V, -3V then the voltage level also same as Nine switch MLI and the simulation of a 7-level 7 switch MLI output waveform shown in Fig 8.

6. CONCLUSION

A new proportioned MLI structure using separate voltage sources and a relatively small number of semiconductor switches compared to the existing MLI topologies has been developed. The number of voltage levels are been obtainfrom the same dc sources in order to achieve a good voltage spectrum. Number of operating switches is been decrease in each step in order to reduce conduction losses and to obtain a higher efficiency. The proposed topology is suitable for photovoltaic, FACTS and UPS applications.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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