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A Buck & Boost based Grid Connected PV Inverter Maximizing Power Yield from Two PV Arrays in Mismatched Environmental Conditions

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ABSTRACT

A single phase grid connected transformerless photo voltaic (PV) inverter which can operate either in buck or in boost mode, and can extract maximum power simultaneously from two serially connected subarrays while each of the subarray is facing different environmental conditions, is presented in this paper. As the inverter can operate in buck as well as in boost mode depending on the requirement, the constraint on the minimum number of serially connected solar PV modules that is required to form a subarray is greatly reduced. As a result, power yield from each of the subarray increases when they are exposed to different environmental conditions. The topological configuration of the inverter and its control strategy are designed so that the high frequency components are not present in the common mode voltage thereby restricting the magnitude of the leakage current associated with the PV arrays within the specified limit. Further, high operating efficiency is achieved throughout its operating range. A detailed analysis of the system leading to the development of its mathematical model is carried out. The viability of the scheme is confirmed by performing detailed simulation studies. A 1.5 kW laboratory prototype is developed, and detailed experimental studies are carried out to corroborate the validity of the scheme.

Keywords : Grid connection, Single phase, Transformerless, Buck & Boost based PV inverter, Maximum power point, mismatched environmental condition, Series connected module.

1. INTRODUCTION

The major concern of a photo voltaic (PV) system is to ensure optimum performance of individual PV modules in a PV array while the modules are exposed to different environmental conditions arising due to difference in insolation level and/or difference in operating temperature. The presence of mismatch in operating condition of modules significantly reduces the power output from the PV array [1]. The problem with the mismatched environmental conditions (MEC) becomes significant if the number of modules connected in series in a PV array is large. In order to achieve desired magnitude for the input dc link voltage of the inverter of a grid connected transformerless PV system, the requirement of series connected modules becomes high. Therefore, the power output from a grid connected transformerless (GCT)Manuscript received July 12, 2017; revised October 10, 2017; accepted October 31,

2017. S. Dutta and K. Chatterjee are with the Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai 400076, India (e-mail: subdut87@gmail.com; kishore@ee.iitb.ac.in). PV system such as single phase GCT (SPGCT) inverter based systems derived from H-bridge [2], [3] and neutral point clamp (NPC) inverter based systems [4], [5] get affected significantly during MEC. In order to address the problem arising out of MEC in a PV system, various solutions are reported in the literature. An exhaustive investigation of such techniques has been presented in [6]. Power extraction during MEC can be increased by choosing proper interconnection between PV modules [6], [7] or by tracking global maximum power point (MPP) of PV array by employing complex MPP tracking (MPPT) algorithm [6], [8]. However, these techniques are not effective for low power SPGCT PV system. Similarly, reconfiguration of the PV modules in a PV array by changing the electrical connection of PV modules [9], [10] is not effective for SPGCT PV system due to the considerable increment in component count and escalation in operating complexity. In order to extract maximum power from each PV module during MEC, attempts have been made to control each PV module in a PV array either by having a power electronic equalizer [11] or by interfacing a dc to dc converter [1], [12]- [14]. Schemes utilizing power electronic equalizer require large component count thereby increasing the cost and operation complexity of the system. The scheme presented in [1] uses generation control circuit (GCC) to operate each PV module at their respective MPP wherein the difference in power between each module is only processed through the GCC. Scheme presented in [12] uses shunt current compensation of each module as well as series voltage compensation of each PV string in a PV array to enhance power yield during MEC. The schemes based on module integrated converter [13], [14] use dedicated dc to dc converter integrated with each PV module. However, the efficiency of the aforesaid schemes are low due to the involvement of large number of converter stages, and further in these schemes the component count is high and hence they face similar limitations as that of power electronic equalizer based scheme. Instead of ensuring MPP operation of each and every module, certain number of modules are connected in series to form a string and the so formed strings are then made to operate under MPP in [15], [16]. Even then there is not much reduction in overall component count and control complexity [6]. In order to simplify the control configuration and to reduce the component count, schemes reported in [17], [18] combine all the PV modules into two subarrays, and then each of the subarray is made to operate at their respective MPP. However,the reported overall efficiency of both the schemes are poor. By introducing a buck and boost stage in SPGCT PV inverter, power extraction during MEC is improved in [19]- [21]. Further, as a consequence of the presence of the intermediate boost stage, the requirement of series connected PV modules in a PV array has become less. In the schemes presented in [19]- [21], the switches of either the dc to dc converter stage or inverter stage operate at high frequency, as a result there is a considerable reduction in the size of the passive element count, thereby improving the operating efficiency of these schemes. Further, the reported efficiency of [20] and [21] is 1-2 % higher than that of [19]. An effort has been made in this paper to divide the PV modules into two serially connected subarrays and controlling each of the subarray by means of a buck and boost based inverter so that optimum power evacuation from the subarrays is ascertained during MEC. This process of segregation of input PV array into two subarrays reduces the number of series connected modules in a subarray almost by half compared to that of the schemes proposed in [20], [21]. The topological structure and control strategy of the proposed inverter ensure that the magnitude of leakage current associated with the PV arrays remains within the permissible limit. Further, the voltage stress across the active devices is reduced almost by half compared to that of the schemes presented in [20], [21], hence very high frequency operation without increasing the switching loss is ensured. High frequency operation also leads to the reduction in the size of the passive elements. As a result the operating efficiency of the proposed scheme is high. The measured peak efficiency and the European efficiency (ηeuro) of the proposed scheme is found to be 97.65% and 97.02% respectively. The detailed operation of the proposed inverter with mathematical validation is explained in Section II. Afterwards the mathematical model of the proposed inverter has been derived in Section III followed by the philosophy of control

strategy in Section IV. The criteria to select the values of the output filter components are presented in Section V. The proposed scheme is verified by performing extensive simulation studies and the simulated performance is presented in Section VI. A 1.5 kW laboratory prototype of the proposed inverter has been fabricated to carry out thorough experimental studies. The measured performances of the scheme which confirm its viability are presented in Section VII.

2. PROPOSED INVERTER AND ITS OPERATION

The schematic of the proposed Dual Buck & Boost based Inverter (DBBI) which is depicted in Fig. 1 is comprising of a dc to dc converter stage followed by an inverting stage. The dc to dc converter stage has two dc to dc converter segments, CONV1 and CONV2 to service the two subarrays, P V1 and P V2 of the solar PV array. The segment, CONV1 is consisting of the self-commutated switches, S1 along with its anti-parallel body diode, D1, S3 along with its anti-parallel body diode, D3, the free wheeling diodes, Df1, Df3 and the filter inductors and capacitors, L1, Cf1, and Co1. Similarly, the segment, CONV2 is consisting of the self-commutated switches, S2 along withits anti-parallel body diode, D2, S4 along with its anti-parallel body diode, D4, the free wheeling diodes, Df2, Df4 and the filter inductors and capacitors, L2, Cf2, and Co2. The inverting stage is consisting of the self-commutated switches, S5, S6, S7, S8, and their corresponding body diodes, D5, D6,D7 and D8 respectively. The inverter stage is interfaced with the grid through the filter inductor, Lg. The PV array to the ground parasitic capacitance is modeled by the two capacitors, Cpv1 and Cpv2

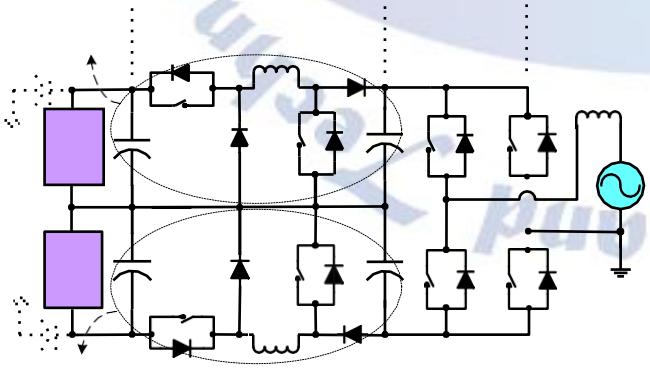


Fig.1.Dual Buc k& Boost based Inverter(DBBI)

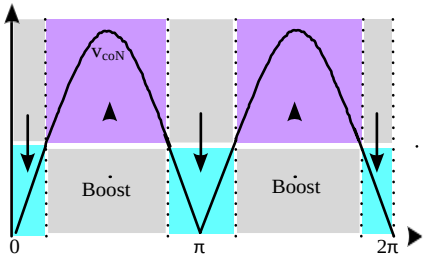
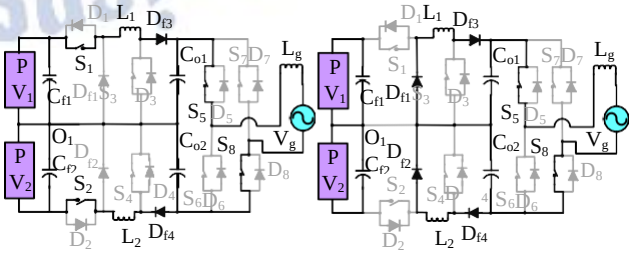


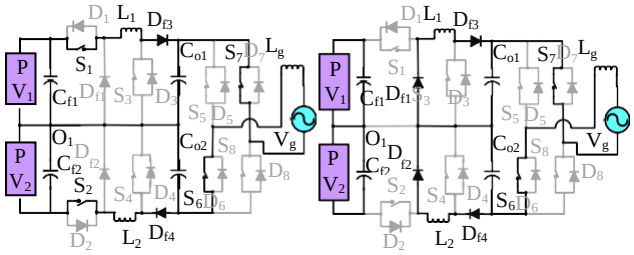
Fig.2.Buck stage and Boost stage of the proposed inverter

Considering Fig. 2, $CONV_1$ operates in buck mode when $V_{pv1} \geq v_{co1}$, while $CONV_2$ operates in buck mode when $V_{pv2} \geq v_{co2}$. V_{pv1}, V_{pv2} are the MPP voltages of PV_1 and $PV_2$and v_{co1}, v_{co2} are the output voltages of $CONV_1$ and $CONV_2$respectively. During buck mode duty ratios of the switches,S_1 and S_2 are varied sinusoidally to ensure sinusoidal gridcurrent (i_g) while S_3 and S_4 are kept off. When $V_{pv1}<v_{co1}$,$CONV_1$ operates in boost mode while $CONV_2$ operates inboost mode when $V_{pv2}<v_{co2}$. During boost mode dutyratios of the switches, S_3 and S_4 are varied sinusoidally toensure sinusoidal $i_g$while S_1 and S_2 are kept on throughoutthis mode. The sinusoidal switching pulses of the switches of$CONV_1$ and $CONV_2$ are synchronized with the grid voltage,$v_g$to accomplish unity power factor operation. The switches,S_5andS_8arekeptonandswitchesS_6andS_7arek eptoff permanently during the entire positive half cycle (PHC)while during entire negative half cycle (NHC), the switches,S_6 and S_7 are kept on and switches, S_5 and S_8 are kept offpermanently. All the operating states of the proposed inverteraredepictedinFig.3.

When the insolation level and ambient temperature of sub-arrayPV_1aredifferentfromthatofPV_2,theMPPpara meters



(a) (b)



(c) (d)

FigOperating states of DBBI: (a) Active and (b) Freewheeling states in buck mode of PHC, (c) Active and (d) Freewheeling states in buck mode of NHC, (e) Active and (f) Freewheeling states in boost mode of PHC, (g) Active and (h) Freewheeling states in boost mode of NHC

of the two subarrays, V_{pv1} andV_{pv2}, MPP current, I_{pv1}andI_{pv2}correspond to PV_1 and PV_2 respectively and power atMPP, P_{pv1} and P_{pv2} correspond to PV_1 and PV_2 respectivelydiffer from each other. By considering that both the subarraysare operating at their respective MPP and neglecting thelosses incurred in power processing stages, the average powerinvolved with $C_{o1}$and C_{o2}, P_{co1} andP_{co2} over a half cyclecan be assumed equal to the power extracted from PV_1 andPV_2.Therefore,

$P_{co}1=P_{pv}1$ &$P_{co}2=P_{pv}2$ (1)

Thepowerinjectedtothegridaveragedoverahalfcycle,P_g canbewrittenas

$$P_g=P_{pv1}+P_{pv}\ (2)$$

Further, at any half cycle

vg = vco1 + vco2 (3)

Hence, the instantaneous injected power to the grid, pg can be written as

pg = vgig = (vco1 + vco2)ig(4)

wherein vco1 and vco2 denote the instantaneous quantities of Vco1 and Vco2 respectively. As ig is in-phase with vg,

Ig = Pg Vg (5)

wherein Vg and Ig denote rms values of vg and ig respectively. The power injected to the grid can be expressed as

Pg = 1 π Z π 0 pg d(ωt) = 1 π Z π 0 vco1ig d(ωt) + 1 π Z π 0 vco2ig d(ωt) (6) = Pco1 + Pco2 (7)

As vco1 and vco2 are synchronized with vg. Hence Pco1 = 1 π Z π 0 Vco1m sin(ωt) Igm sin(ωt) d(ωt) = Vco1mIgm 2 (8)

Similarly, Pco2 = Vco2mIgm 2 (9)

wherein the amplitudes of vco1, vco2 and ig are denoted as Vco1m, Vco2m and Igm respectively. Combining (1), (8) and (9)

Vco1m = 2Ppv1 Igm = √ 2Ppv1 Ig = √ 2Ppv1 Pg/Vg (10)

Vco2m = 2Ppv2 Igm = √ 2Ppv2 Ig = √ 2Ppv2 Pg/Vg (11)

Similarly by combining (2), (10) and (11),

Vco1m = VmPpv1 Ppv1 + Ppv2 & Vco2m = VmPpv2 Ppv1 + Ppv2 (12)

The voltage templates of vco1 and vco2 appear as full wave rectified sinusoidal waveform with amplitudes, Vco1m and Vco2m respectively. Vm is the amplitude of vg. It can be deduced from (12) that the magnitudes of Vco1m and Vco2m are decided by the power extracted from each of the subarray. If the power extracted from P V1 is less than P V2, then Vco1m < Vco2m, whereas Vco2m < Vco1m if power extracted from P V2 is less than P V1. During buck mode, the duty ratios, d1 of S1 and d2 of S2 vary sinusoidally with an amplitude d1m and d2m,

wherein d1m = Vco1m Vpv1 & d2m = Vco2m Vpv2 (13) while during boost mode the duty ratios, d3 of S3 and d4 of S4 vary sinusoidally with amplitude d3m and d4m,

wherein d3m = 1 − Vpv1 Vco1m & d4m = 1 − Vpv2 Vco2m (14)

The CONV1 and CONV2 are having the same output current ig. Hence, the input side currents before getting filtered by input filter capacitors of CONV1, isw1 and CONV2, isw2 can be related with ig in the buck mode by considering the switching cycle average of corresponding quantities as follows hisw

1iTs = hd1iTs higiTs (15)

hisw2iTs = hd2iTs higiTs (16)

Similarly, by considering switching cycle average of corresponding quantities the relation between isw1,

isw2 and ig can be deduced during boost mode as

hisw1iTs = h 1 1 − d3 i Ts higiTs (17)

hisw2iTs = h 1 1 − d4 i Ts higiTs (18)

Therefore, it can be inferred from (12) and (13) that if the insolation level of P V1 is lower than that of P V2, during buck mode, d1m < d2m, thereby hd1iTs < hd2iTs whereas during boost mode as per (12) and (14), d3m < d4m, thereby hd3iTs < hd4iTs . Hence, it can be concluded from (15), (16), (17) and (18) that in any operating mode, hisw1iTs < hisw2iTs , therefore Ipv1 < Ipv2. Following the same argument, Ipv1 > Ipv2 if the insolation level of P V1 is higher than that of P V2. Considering Fig. 1 it can be noted that during operation in PHC, vcpv1 = vco2 + Vpv1, vcpv2 = vco2 − Vpv2 whileduring NHC $v_{cpv}1 = v_{co}1 + V_{pv}1$, $v_{cpv}2 = v_{co}1 V_{pv}2$,wherein v_{cpv1} and v_{cpv2} are the voltages impressed acrossC_{pv1} and C_{pv2} respectively. Hence, the voltages across C_{pv1}andC_{pv2}containsignificantamountofdcandlowfrequencycomponents which also ensures that the magnitude of theleakage current is maintained within the limit specified in thestandard,VDE0126-1-1,andalsocitedin[23].

3. CONTROL STRATEGY OF THE PROPOSED SCHEME

The control strategy of the proposed scheme is depicted in Fig. 5. The controller is designed to fulfill the following objectives: i) both subarrays operate at their corresponding MPP simultaneously, ii) sensing of output voltages, vco1 and vco2 are not required, iii) ig is sinusoidal and is in-phase with vg throughout the operating range. Two separate MPP trackers and two proportional integral (PI) controllers are employed to determine the value of Ppv1 and Ppv2 which are requiredto estimate Vco1m and Vco2m. Using (12), Vco1m and Vco2m are determined where the information of Vm is obtained from the phase locked loop (PLL). A rectified version of a unity sinusoidal function, R is generated from a unity sinusoidal function, X, synchronized with vg, and is obtained from the same PLL. R is multiplied with Vco1m and Vco2m to estimate vco1 and vco2. Hence, two voltage sensors which otherwise would have been required to determine vco1 and vco2 get eliminated. Vpv1 and vco1 are compared to decide about the mode of operation (buck mode or boost mode) of CONV1, while Vpv2 and vco2 are compared to determine the mode of operation of CONV2. RMS values of vco1 and vco2 are estimated which are then subsequently squared and are then divided by Ppv1 and Ppv2 to obtain the emulated effective resistances, Rpco1 and Rpco2 of the two component converters. Subsequently the reference current, iL1ref of L1 and the reference current, iL2ref of L2, are synthesized by utilizing (28) in the buck mode [21],

iL1ref = vco1 Rpco1 and iL2ref = vco2 Rpco2 (28)

while for boost mode (29) is used to generate iL1ref and iL2ref [21].

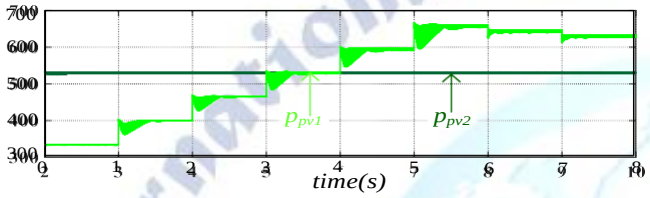
iL1ref = v 2 co1 Rpco1Vpv1 and iL2ref = v 2 co2 Rpco2Vpv2 (29)

The sensed inductor currents, iL1 and iL2 are compared with their corresponding references iL1ref and iL2ref . The errors so obtained are processed through two separate PI controllers to generate the required sinusoidal duty ratios for the switches, S1 and S2 during buck mode. Similarly, two separate PI controllers are engaged to process the generated errors to synthesize required sinusoidal duty ratios for switches S3 and S4 during boost mode. Signal Y is used to generate gating signals for S5, S8 while signal Z is used to generate gating signals for S6, S7 of the grid frequency unfolding inverter.

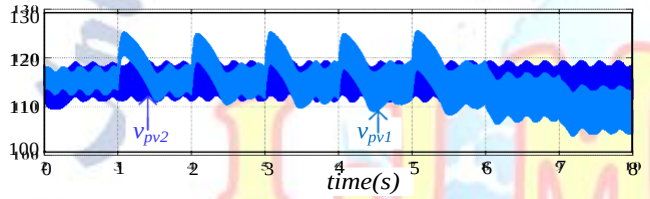
4. SIMULATION STUDY

To demonstrate the efficacy of the proposed inverter a PV array consisting of two PV subarrays while each of the subarray having four series connected Canadian solar polycrystalline modules 'CS6P-165PE' [25] is considered. The MPP parameters of each subarray at standard test condition (STC) are as follows: Vpv1 = Vpv2 = 116 V, Ipv1 = Ipv2 = 5.7 A and Ppv1 = Ppv2 = 661 W. The parameters which are used to simulate the proposed inverter are indicated in Table I. MATLABSimulink platform is utilized to simulate the performance of the proposed inverter.The variation in insolation level and temperature with respect to time which is considered for the two subarrays to demonstrate the effectiveness of the proposed inverter are tabulated in Table II. Estimated variation of Ppv1, Ppv2 along with the other parameters Igm, Vco1m, Vco2m, peak of iL1 (IL1m) and peak of iL2 (IL2m) are also indicated in the same table. Fig. 6(a)-(c) represents

the variation of Ppv1, Ppv2, Vpv1, Vpv2, Ipv1, Ipv2 of the two subarrays and also demonstrate the ability of the proposed inverter to operate the two subarrays simultaneously at their respective MPP. Variation in ig, iL1, iL2, vco1 and vco2 along with their magnified versions for two different insolation levels are depicted in Figs. 7 to 9. The estimated values of the aforementioned quantities as tabulated in Table II conform to that of obtained through simulation studies thereby ensuring the viability of the proposed scheme.



(a)



(b)

Simulated waveform: Variation in (a) ppv1 and ppv2, (b) vpv1 and vpv2

5. EXPERIMENTAL VERIFICATION

A 1.5 kW laboratory prototype of the proposed inverter is fabricated and detailed experimental studies have been carried out to demonstrate the effectiveness of the proposed scheme. The photograph of the experimental prototype is shown in Fig. 10. Buck stage Boost stage Inverting stage Sensing board Buffer circuit Driver Fig. 10. Experimental prototype of the proposed inverter The EPS PSI9306-15 power supply has the provision to change only the effect of insolation level while the option to change the effect of temperature is unavailable. In order to emulate simultaneous variation in temperature and level of insolation, the MPP parameters of the two solar emulators (solar emulator 1 as P V1 and solar emulator 2 as P V2) are set as follows at STC: Vpv1 = 130 V, Ipv1 = 5 A and Vpv2 = 120 V, Ipv2 = 5 A. The variation in insolation level of P V1 is indicated in Table III while the insolation level of P V2 is maintained at 80%. The expected values of Ipv1, Ipv2, Ppv1, Ppv2, Vco1m, Vco2m, Igm, IL1m, IL2m for the entire operating range are tabulated in the Table III. Fig. 11 depicts the change in ig, Ipv1, Ipv2, Ppv1, Ppv2 throughout the range of variation in the level of insolation as specified in Table III. Magnified version of the responses of vco1, vco2, iL1 and iL2 along with vg, ig are also shown in Fig. 12(a) to (f) for two different insolation levels of P V1. The figures Fig. 12(a) and (b) ensure that ig remains to be sinusoidal and in-phase with vg in spite of having difference in the magnitude of power being extracted from the two subarrays. From Fig. 12(c) it can be inferred that the converter associated with P V1 operates completely in buck mode, whereas the converter associated with P V2 operates in both buck and boost mode depending on the requirement. Thus, it can be inferred that the two converter segments are able to operate in a decoupled fashion. The measured variables, Ipv1, Ipv2, Ppv1, Ppv2, Vco1m, Vco2m, Igm, IL1m, IL2m as depicted in Figs. 11, 12 are more or less same as that of the estimated ones presented in Table III, and this validates the ability of the proposed inverter to extract maximum power from twosubarrays operating under MEC.

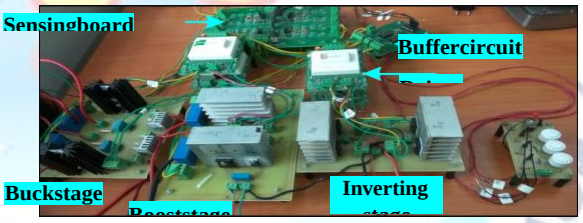


Fig Experimental prototype of the proposed inverter

Fig Shows depictsthe FastFourier Transform (FFT) o fig. The THD of igis found to be 4.61% which is below the limit of5% as specified in the standards, IEEE 1574/IEC 61727 [22].It may be noted that the measured THD of vgis found to be2.12% and hence the contribution to THD from the inverter ismuchlessthan4.61%.

The measured and estimated efficiency curves of the proposed inverter are shown Fig.14. In order to measure the efficiency of the proposed inverter the Yokogawa make power analyzer, WT1800 is used and further, the losses incurred in the active and passive elements of the power circuit is considered while the losses involved with the control circuit are neglected. The efficiency is determined while both Vpv1 and Vpv2 are set at 130 V. Measured peak efficiency is found to be

97.65% and the measured European efficiency (ηeuro) is obtained as 97.02%.

6. CONCLUSION

A single phase grid connected transformerless buck and boost based PV inverter which can operate two subarrays at their respective MPP was proposed in this paper. The attractive features of this inverter were i) effect of mismatched environmental conditions on the PV array could be dealt with in an effective way, ii) operating efficiency achieved, ηeuro = 97.02% was high, iii) decoupled control of component converters was possible, iv) simple MPPT algorithm was employed to ensure MPP operation for the component converters, v) leakage current associated with the PV arrays was within the limit mentioned in VDE 0126-1-1. Mathematical analysis of the proposed inverter leading to the development of its small signal model was carried out. The criterion to select the values of the output filter components was presented. The scheme was validated by carrying out detailed simulation studies and subsequently the viability of the scheme was ascertained by carrying out thorough experimental studies on a 1.5 kW prototype of the inverter fabricated for the purpose

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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