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High power application driven by 9-Level ANPC inverter using SVM- based control

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ABSTRACT

Active neutral point is the most attractive inverter topology in many applications such as a photovoltaic system and wind energy systems because of the equal loss distribution among switches. This study presents a new single-phase nine-level active neutral-point clamped converter topology. It can be applied to achieve optimal total harmonic distortion. In addition, this topology helps to obtain voltage balancing among the capacitors. An analysis of the switching state and commutation of the converter are also presented here in order to balance the power losses among the semiconductor devices.

The nine-level active neutral-point-clamped (9LANPC) converter has been widely studied for its excellent performance in high-power medium-voltage applications. This paper analyzes the space vector pulse width modulation (SVPWM) strategy of the 9L-ANPC converter in the virtual coordinate, and presents an optimized control strategy which can balance the neutral point (NP) voltage and avoid the dead-time effects for the first time. The simulation has been carried out in MATLAB SIMULINK to investigate the effectiveness of the proposed topology.

Key Words: ANPC, THD, Multilevel Inverter, SVPWM.

1. INTRODUCTION

Neutral-point clamped (NPC) is the most well-known multilevel configuration. It is widely used in photovoltaic and wind turbine applications because of the following advantages it offers [2].

- It has lower dv/dt.
- Less voltage stress on the switches.
- Reduction of total harmonic distortion (THD) of output and common mode current is possible

However, the most common disadvantage of NPC topology is voltage imbalance among the series capacitors. In many studies the balancing problem of multilevel three phases diode-clamped was the main focus. However until now the only solution that has been implemented is for high modulation indices. Balancing is not possible unless additional hardware is used for balancing the voltage as the number of levels increases in the converter. Another drawback is unequal distribution of losses among semiconductor devices. This characteristic reduces the maximum output power and reduces the converter efficiency. To maintain equal distribution of losses among switches devices the three-level active neutral-point clamped (3L-ANPC) converter is considered the best choice [1]. Since the

introduction of the 3L-ANPC great deal of attention has been given to multilevel converters topologies. To achieve optimal THD active neutral-point clamped five-level (ANPC-5 L) has been proposed. However, the capacitors voltage balancing is a crucial task in ANPC and the control is also more complex. To maintain the voltage of the capacitors in the dc link, numerous redundancies are used in [8] to control the capacitors voltage. Such topology contributes to increasing the inverter output voltage levels and enhances the power.

This paper presents a novel single-phase 9L-ANPC for low-voltage applications. The waveform profile of the inverter output is close to a pure sine wave. A technique to make the voltage in dc-link capacitors balanced has been proposed.

To ensure the equal distribution of switching losses two pulse-width modulation (PWM) strategies are used and compared with each other. A brief comparison between the proposed inverter and other counterparts is carried out. Finally, simulation and experimentation results are provided to ensure the feasibility of the proposed inverter and the employed modulation techniques.

2. PROPOSED CONVERTER:

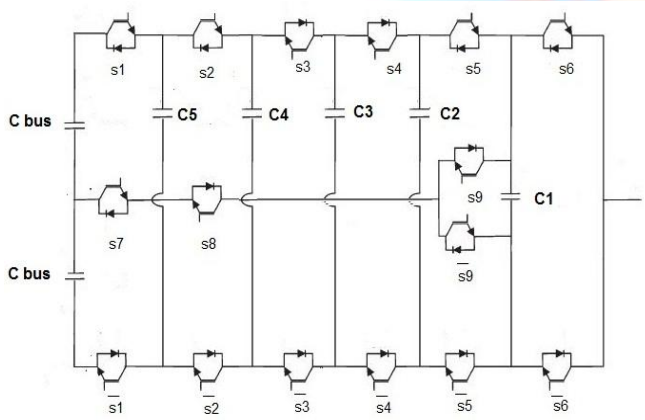

Fig 1: Proposed Nine-Level ANPC configuration

The new 9L-ANPC converter is presented in Fig. 1. It combines features from the NPC and the FC topologies resulting in two main advantages:

- It only uses one neutral point (NP) like the 3L-NPC, which makes it capable of operating in the four quadrants. A neutral point voltage balance study for the new 9L-ANPC converter has been carried out as it is done in [10] for the 3L-NPC, obtaining the curve of Fig. 3. At any point below the curve the neutral point can be controlled each switching period and above the curve a voltage ripple at three times the fundamental frequency appears. In any case, the voltage ripple is controllable at any point using a Nearest Three Vectors (NTV) modulation. This characteristic is independent of the topology and common to multilevel topologies with one neutral point, that is, it can be observed in the 3L-NPC, in the previously employed 5L-ANPC and in the proposed 9L-ANPC converter.
- The volume required by the flying capacitors is reduced in comparison to the FC topology, making the construction of the converter feasible. Furthermore, the C1 flying capacitor of the new topology is dimensioned like the C1 capacitor of the previously employed 9L-ANPC. C2, C3, C4 and C5 capacitors are much smaller comparing to C1, their size is similar to the size of a decoupling capacitor and no control is required to maintain their voltages at their rated values [6]. Thus, the new 9L-ANPC requires the same number of voltage sensors to control the topology as the previously employed 9L-ANPC (VC1, VDC and NP voltage).

  The previously employed 9L-ANPC also features these advantages. However, the new 9L-ANPC has two main advantages over the previous 9L-ANPC.

  It does not require any series connection of semiconductors, whereas the previous topology connects semiconductors in series and requires additional hardware [6] to hold their blocking voltage at their rated value. C1, C2, C3, C4, and C5 assure the desired blocking voltage value of all semiconductors in the new topology.

Operating principle:

The new converter has 5 voltage levels (+VDC/2, +VDC/4, +VDC/6, +VDC/8, 0, -VDC/8, -VDC/6, -VDC/4 and -VDC/2). The operation of the new converter can be divided in two distinct half-periods: the positive and negative half-period of the output voltage. During the positive output voltage half-period, CBUS1 and C1 are used to obtain +VDC/2, +VDC/4, +VDC/6, +VDC/8, 0 voltages and during the negative output voltage half-period [1], CBUS2 and C1 are used to obtain 0, -VDC/8, -VDC/6, -VDC/4 and -VDC/2 voltages [2]. Each half period can be identified with an inner 3L-FC, as shown in Figure 2. Dotted polygon delimiters the inner

3L-FC for the positive half-period and the dashed polygon delimiters the inner 3L-FC for the negative half-period. S7 switches at fundamental frequency similarly to S1 in the previously employed 5L-ANPC.

During the positive output voltage half-period +VDC/8 can be obtained adding the C1 voltage (VC1) to the NP or subtracting VC1 to +VDC/2. These two different switching states have opposite effects on VC1. In the same way, during the negative output voltage half-period -VDC/8 can be obtained adding VC1 to -VDC/2 or subtracting VC1 to the NP. These two different switching states have also opposite effects on VC1. Therefore, VC1 can be kept under control by choosing the appropriate switching states [3].

3. MODULATION TECHNIQUE OF 9L-ANPC SYSTEM:

In this section a simple modulation technique is described to control the new 9L-ANPC converter for a three phase system. The modulation is based on that described in [7], but in our case, the space vector modulation (SVM) technique is used instead of the carrier-based PWM. A sixth part of the vector diagram for a nine-level converter is shown in Figure 3, where +VDC/2, +VDC/4, +VDC/6, +VDC/8, 0, -VDC/8, -VDC/6, -VDC/4 and -VDC/2 voltage levels are denoted as 8, 7, 6, 5, 4, 3, 2, 1 and 0 respectively [4].

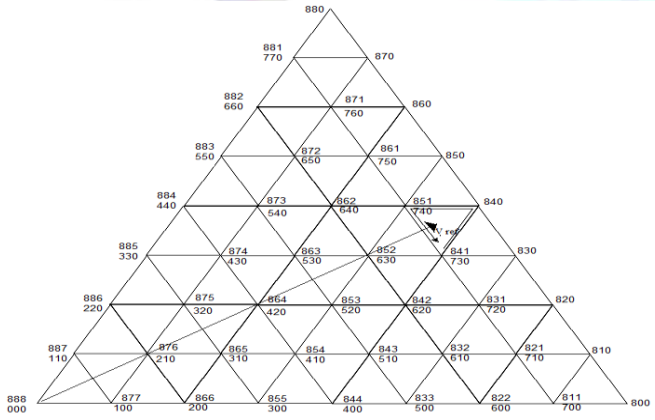

Fig 3: vector diagram for 9Level converter

The modulation and the control technique comprises in different stages such as:

1. Depends on the reference value of phase angle and modulation index consider the nearest three possible vector components.
2. Choose a sequence consists of four vectors as {x1, x2, x3, and x4} in this the first and last vectors are similar. From the figure 3 consider the sequence of four vectors as {(841), (840), (740), (730)}. And from this the duty cycles are obtained as {d1, d2 and d3} [9].

4. SIMULATION DIAGRAM AND EXPLANATIONS:

In this paper the figure 4 shows the simulation experimental diagram for the nine level Active Neutral Point Clamped technique based on the figure1. The gate signals for this converter is obtained by the space vector method.

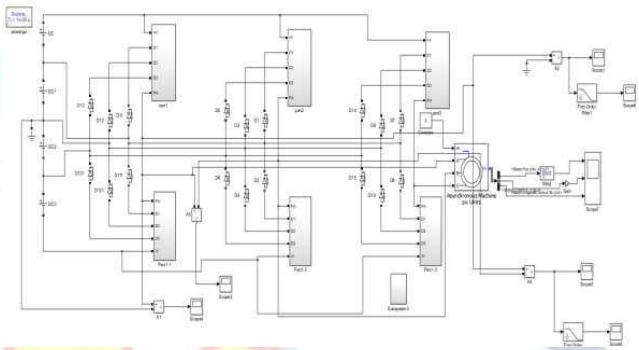

Figure 4: Simulation Diagram for the ANPC system

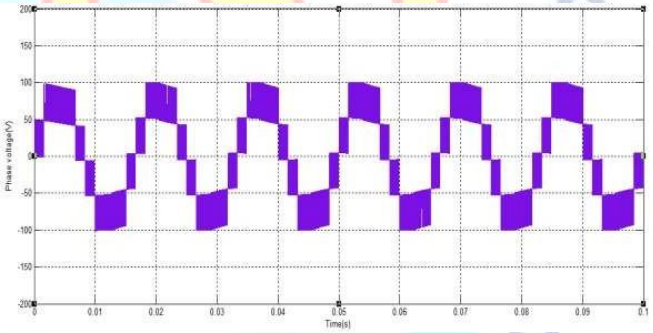

Figure 5: Waveform shows a Phase voltage without filter

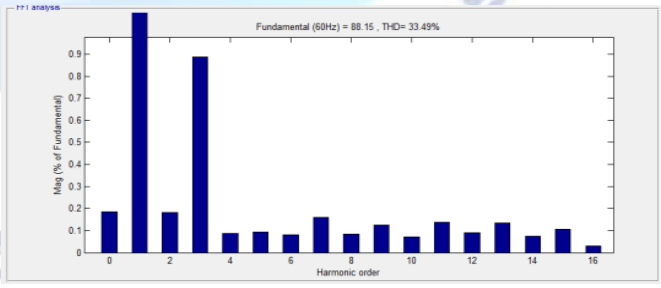

Figure 6: THD of hase voltage without filter

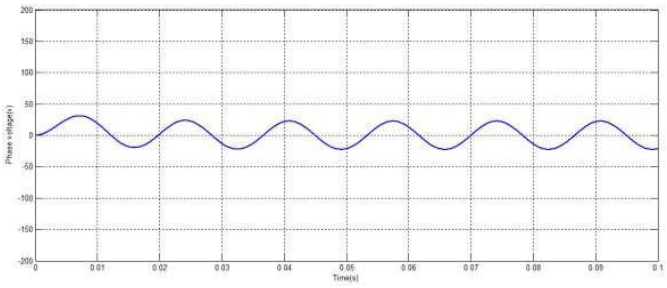

Figure 7: Waveform shows a Phase voltage with filter

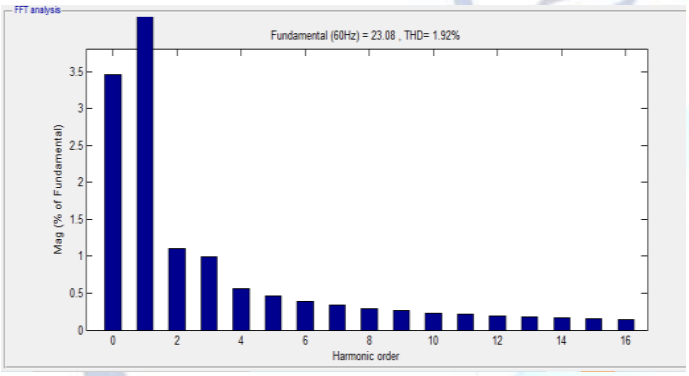

Figure 8: THD of Phase voltage with filter

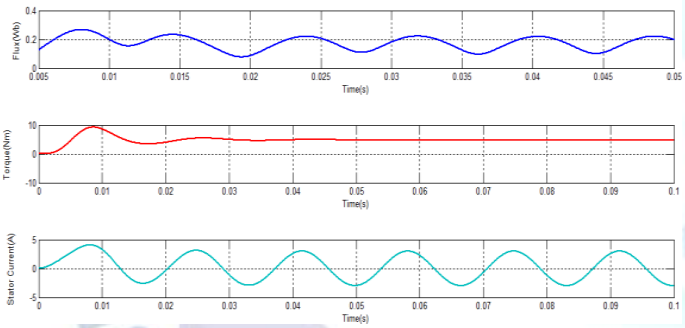

Figure 9: Waveform shows a flux, Torque, Stator Current

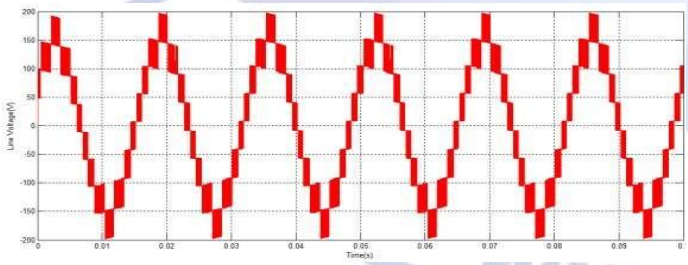

Figure 10: Waveform Shows a Line voltage without filter

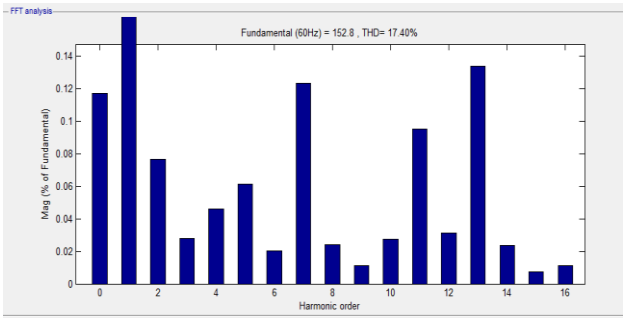

Figure 11: THD of Line voltage without filter

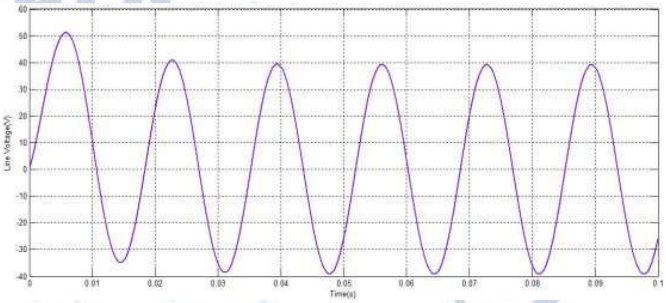

Figure 12: Waveform shows a Line Voltage with filter

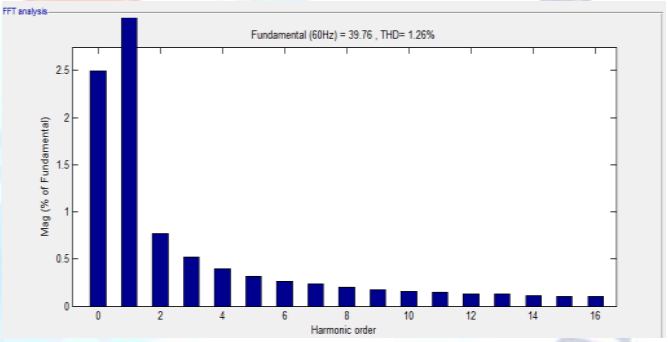

Figure 13: THD of Line voltage with filter

A. Table 1: Comparative analysis

THD Parameter	3-Level	9-Level
Output Voltage Without Filter	33.49%	17.40%
Output Voltage Without Filter	1.92%	1.26%

5. CONCLUSION:

This paper presents an optimized control strategy based on the well-known SVPWM for 9L-ANPC converters. The proposed strategy analyzes all the space vectors' characteristics of balancing the NP voltage, and

divides them into seven categories of triangles. Every category has its own principles to choose the vector sequence and compute the vector durations based on the NP voltage difference, which can balance the NP voltage flexibly. This optimized control strategy also provides principles to choose appropriate switching states for voltage levels to make sure that the No-Offset-Glitches of phase voltages can be avoided successfully. A low power three-phase 9L-ANPC converter prototype is built to verify the performance of the optimized control strategy.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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