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Design Methodologies and Strategies for Low Power VLSI

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ABSTRACT

Low power has emerged as a principal theme in today's world of industries. Power dissipation has become an awfully necessary thought as performance and area for VLSI Chip vogue. With shrinking technology reducing power consumption and over all power management on chip square measure the key challenges below 100nm because of enlarged complexity. For many designs, optimization of power is extremely necessary as temporal property because of the requirement to cut back package value and extended battery life. For power management run current to boot plays an awfully necessary role in low power VLSI designs. Leak current is popping into associate a lot of and a lot of necessary fraction of the total power dissipation of integrated circuits. This paper describes regarding the various strategies, methodologies and power management techniques for low power circuits and systems. Future challenges that got to be met to designs low power high performance circuits square measure conjointly mentioned.

KEYWORDS: *Power Dissipation, low power, process nodes, leakage current, split level charge recovery logic, efficient charge recovery logic, positive feedback adiabatic logic ,power management*

I. INTRODUCTION

The advantage of utilizing a mix of low-power parts in conjunction with low-power design techniques is additional valuable currently than ever before. Needs for lower power consumption Continue to increase considerably as parts become powered, smaller and need additional functionality. Within the past the most important issues for the VLSI designers was space, performance and price. Power thought was the secondary involved. Currently a day's power is that the primary involved due to the exceptional growth and success within the field of private computing devices and wireless communication system that demand high speed computation and sophisticated practicality with low power consumption. The motivations for reducing power consumption disagree application to application. Within the category of micro-powered battery operated transportable applications like cell phones; the goal is to stay the battery period of time and weight affordable and packaging value low.

For high performance transportable computers like laptop computer the goal is to cut back the ability dissipation of the electronics portion of the system to some extent that is regarding 1/2 the overall power dissipation. Finally for the high performance non battery operated system like workstations the goal of power minimization is to cut back the system value whereas making certain long run device reliableness. For such high performance systems, method technology has driven power to the fore front to any or all factors in such designs. At method nodes below one hundred nm technology, power consumption thanks to leak has joined switching activity as a primary power management concern. There square measure

several techniques [15] that have been developed over the past decade to handle the unendingly aggressive power reduction requirements of most of the high performance. the fundamental low-power style techniques, like clock gating for reducing dynamic power, or multiple voltage thresholds (multi-Vt) to decrease leak current, square measure well-established and supported by existing tools [17]. From figure one we are able to analyze however many changes takes place in circuit style mistreatment power dissipation [15].

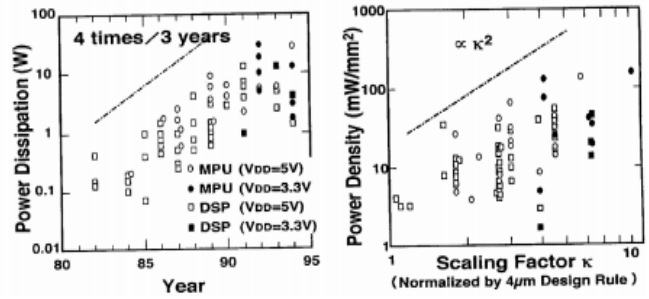

Figure 1: Evolution in Power dissipation

II. LOW POWER STRATEGIES

There (table-1) are different strategies available at different level in VLSI design process for optimizing the power consumption: Table -1, Strategies for low power designs

Design Level	Strategies
Operating System Level	Portioning, Power down
Software level	Regularity, locality, concurrency
Architecture level	Pipelining, Redundancy, data encoding
Circuit /Logic level	Logic styles, transistor sizing and energy recovery
Technology Level	Threshold reduction, multi threshold devices

Effective power management is possible by using the different strategies at various levels in VLSI Design process. So designers need an intelligent approach for optimizing power consumptions in designs. .

III. POWER DISSIPATION BASICS

In a circuit 3 elements area unit answerable for power dissipation: dynamic power, short-circuit power and static power. Out of those, dynamic power or change power is primarily power dissipated once charging or discharging capacitors and is represented below [5, 6]:

$$Pdyn = CL\ Vdd2\ a\ f \qquad (1)$$

Where CL : Load Capacitance, a perform of fan-out, wirelength, and semiconductor device size, Vdd: provide Voltage, that has been dropping with ordered method nodes, α: Activity issue, that means however often, on average, the wires switch, f :Clock Frequency, that is increasing at every ordered process node. Static power or leak power may be a perform of the availability voltage (Vdd), the change threshold (Vt), and semiconductor device sizes (figure2). As method nodes shrink, leak becomes a additional significant supply of energy use, overwhelming a minimum of half-hour of total power [2]. Crowbar currents, caused when each the PMOS and NMOS devices area unit at the same time on, additionally contribute to the leak power dissipation [17]. Most circuit level reduction techniques focus solely on Sub threshold leak reduction while not considering the results of gate leak [15] .For this MTCMOS theme [4] has been projected for reduction of subthreshold leak current in sleep mode. Figure-2 shows the various elements answerable for power dissipation in CMOS.

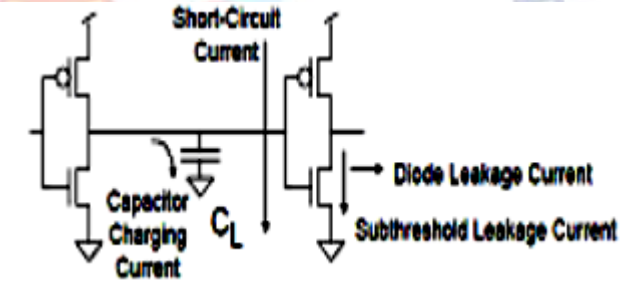

Figure 2, Power Dissipation in CMOS

IV. LOW POWER DESIGN SPACE

From the on top of section it's unconcealed that there area unit 3 degrees of freedom within the VLSI style area : Voltage, Physical Capacitance and information activity. Optimizing for additional power entails a shot toreduce one or additional of those factors. This section in short describes concerning their importance in power optimization method.

4.1Voltage:- thanks to its quadratic relationship to power , voltage reduction offers the foremost effective suggests that of minimizing power consumption.Without requiring any special circuits and technologies, an element of 2 reduction in offer voltage yields an element of 4 decreases in powerconsumption. sadly, there's speed penalty for offer voltage reduction and delays drastically increase as Vdd approaches to the brink voltage VT of the device. The approach to cut back the supply voltage while not loss in turnout is to switch the brink voltage of the devices. Reducing

the VT permits the availability voltage to be scaled down while not loss in speed.The limit of however low lowthe VT will go is ready by the reqirement to line adequate noise margins and management the rise within thesubtreshold outpouring current [6,8,10].

4.2Physical Capacitance:- Dynamic power consumption depends linearly on the physical capacitance being switched. So, additionally to in operation at low voltages, minimizing capacitances offer another technique for minimizing power consumption.The capacitances will be unbroken at aminimum by mistreatment less logic, smaller devices , fewer and shorter wires[6,8,10]. like voltage, however, we tend to aren't unengaged to optimize capacitances severally, as an example reducing device sizesreduces physical capacitance, however it additionally reduces the present drive of the electronic transistor creating the circuit operate additional slowly.

4.3Switching Activity:- There area unit 2 elements to switch activity : Fclk that determines the average periodicityof information arrivals and E(sw) that determines what percentage transitions every arrival can generate[14]. E(sw) is reduced by choosing correct algorithms design improvement, by proper choice of logic topology and by logic level improvement which ends up in less power[15]. The data activity E(sw) area unit combined with the physical capacitance C to obtained switch capacitanceCsw=C.E(sw),which describes the typical capacitance charge throughout every information period1/Fclk thatdetermines the facility consumed by CMOS circuit[9].

V. POWER MINIMIZATION TECHNIQUES

5.1 Reducing Chip and package capacitance: - this may be achieved through method development like SOI with part or absolutely depleted wells, CMOS scaling to submicron device sizes and advanced interconnect substrates like multi chip module (MCM). This approach is very effective however is additionally terribly high-ticket [15, 19].

5.2 Scaling the provision voltage (Voltage Scaling): - This approach is terribly effective in reducing the facility dissipation, however typically needs new IC fabrication process [13].

5.3Using power management strategies: -
Effective power management involves choice of the correct technology, the employment of optimized libraries, IP (intellectual property), and style methodology [1, 19]. Figure-3 shows the effective power management strategy.

5.3.1The Role of Technology Selection: - correct technology choice is one among the key aspects of power management [1]. The goal of every technology advancement is to enhance performance, density, and power consumption. the standard approach in developing a brand new generation of technology is to use constant-electric-field scaling. method designers scale each the applied voltage and therefore the oxide thickness to keep up an equivalent field of force [13,16]. This approach reduces power by regarding 50% with each new technology node but, because the voltage gets smaller, the edge voltage additionally must scale all the way down to meet the performance targets of that technology. This scaling sadly increases the subthreshold current and therefore the outflow power. to beat this constraint, process engineers not apply constant-field scaling for processes of sixty five nm or smaller; instead, they used a a lot of generalized type of scaling. as a result of it's not possible to optimize a technology for each performance and outflow right away, every technology sometimes has 2 variants. One variant aims for prime performance, and therefore the alternative shoots for low outflow. the first variations between the 2 ar within the oxide thickness, provide voltage, and threshold voltage. The technology variant with the thicker gate oxide aims for low-leakage style and should support a better voltage to realize an affordable performance [9]. once choosing a technology to optimize the facility for a given style, you must take each aspects into consideration: the requirement to use a smaller pure mathematics to cut back active power and the need to use a low-leakage variant to cut back outflow.

VI. CONCLUSION

The need for lower power systems is being driven by many market segments. Unfortunately designing for low power adds another dimension to the already complex design problem and the design has to be optimized for power as well as Performance and Area. In conclusion various issues and major challenges regarding low power designs are:-

6.1 Technology Scaling: - It relates with the following factors like: Capacitance per node reduces by 30%, Electrical nodes increases by 2X, Die size grows by 14% (Moore's Law), Supply

Voltage reduces by 15% and Frequency Increases by 2X. To meet these issues relatively 2.7 X active power will increase.

6.2 Leakage power: - To meet frequency demand Vt will be scaled which results high leakage power. A low voltage / low threshold technology and circuit design approach, targeting supply voltage around 1V and operating with reduced thresholds.

6.3 Dynamic power management techniques, varying supply voltage and execution speed according to the activity measurement.

6.4 Low power interconnect, using advance technology, reduced swing or activity approach.

6.5 Development of power conscious techniques and tools for behavioral synthesis, logic synthesis and layout optimization.

6.6 Power saving techniques that recycle the signal energies using the adiabatic switching principals rather them dissipating them as a heat and promising in certain applications where speed can be trades for low power.

REFERENCES

[1] Michael Keating, David Flynn, Robert Aitken, Ala Gibsons and Kaijian Shi, "Low Power Methodology Manual for System on Chip Design", Springer Publications, New York, 2007.

[2] Creating Low-Power Digital Integrated Circuits The Implementation Phase, Cadence, 2007.

[3] Liu, Weidong, Xiaodong Jin, Xuemei Xi, James Chen, Min-Chie Jeng, Zhihong Liu, Yuhua Cheng, Kai Chen, Mansun Chan, Kelvin Hui, Jianhui Huang, Robert Tu, Ping K Ko, and Chenming Hu, BSIM3v3.3 MOSFET Model User's Manual, Department of Electrical Engineering and Computer Sciences, University of California-Berkeley, 2005.

[4] Glasser, Lance A, and Daniel W Dobberpuhl, TheDesign and Analysis of VLSI Circuits, Addison-Wesley Publishing Co, 1985.

[5] Shekar Borkar, "Design Challenges of Technology Scaling," IEEE Micro, July/August 1999, pg 23.

[6] T. Inukai, et.al, "Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve LeakageFree Giga- Scale Integration," Proc. CICC 2000, pp.409-412.

[7] F.Hamzaoglu and M. Stan, "Circuit-Level Techniques to Control Gate Leakage for sub 100nm CMOS," Proc. ISLPED, pp. 60-63, Aug. 2002.

[8] Y. Yeo, et.al, "Direct Tunneling Gate Leakage Current in Transistors with Ultrathin Silicon Nitride Gate Dielectric," IEEE Electron Devices Letters, vol.21, no.11, pp. 540-542, Nov.2000.

[9] S. Mutoh, et.al, "1-V Power Supply High-Speed Digital Circuit Technology with Multi-Threshold Voltage CMOS,"IEEE Journal of Solid State Circuits, vol. 30, no. 8, pp. 847-854, Aug. 1995.

[10] M.Alidina, j. Monterio, S. Devadas, A.Ghosh and M. Papaefthymiou. "Precomputation –based Sequential logic optimization for low power" In Proceedings of the 1994 International Workshop on Low Power Design, pages 57-62, April 1994.

[11] Anand Iyer, "Demystify power gating and stop leakage cold", Cadence Design Systems, Inc.

[12] De-Shiuan Chiou, Shih-Hsin Chen, Chingwei Yeh, "Timing driven power gating", Proceedings of the 43rd annual conference on Design automation,ACM Special Interest Group on Design Automation, pp.121 - 124, 2006.

[13] B.Perman, "Design technologies for VLSI design", encyclopedia of computer science,1995.

[14] Mentor Graphics, "Low power physical design with Olympus SOC", Place and route white paper, March 27, 2009.

[15] Rahul. M.Rao, Jeffery L.Burns, Richard B.Brown, "Circuit Techniques for gate and subthreshold leakage minimization in future CMOS technologies" Proc. ISLPED, pp70-73, 2002.

[16] J.kao, Siva Narendra, Ananta Chandra Kasan, "Subthresh leakage modeling and reduction technique", 2002.

[17] Prasad Subramanian, "Power management for optimal power design", ESILICON, Corp.2010.