International Journal for Modern Trends in Science and Technology
Volume 9, Issue 08, pages 108-115
ISSN: 2455-3778 online
Available online at: http://www.ijmtst.com/vol9issue08.html
DOI: https://doi.org/10.46501/IJMTST0908017

Common Mode Voltage Reduction in 3-Phase VSI with GSPWM Technique

Burra Ashwini | Dr. B. Ravi Chandra Rao

Department of Electrical and Electronic Engineering, G. Narayanamma Institute of Technology & Science, Hyderabad, India.

To Cite this Article
Burra Ashwini | Dr. B. Ravi Chandra Rao. Common Mode Voltage Reduction in 3-Phase VSI with GSPWM Technique. International Journal for Modern Trends in Science and Technology 2023, 9(08), pages. 108-115. https://doi.org/10.46501/IJMTST0908017

Article Info
Received: 28 July 2023; Accepted: 26 August 2023; Published: 27 August 2023.

ABSTRACT

Recent research has focused on improving induction motor drive performance due to the growing need for energy-efficient and dependable motor drives. Their functionality relies on minimizing common mode voltage (CMV) during pulse width modulation (PWM). CMV causes electromagnetic interference and threatens motor insulation. Space Vector Pulse Width Modulation (SVPWM), Active Zero State PWM (AZSPWM), and Near State PWM (NSPWM) are compared in this research to reduce CMV in induction motor drives. The study includes theoretical research and simulation validation. This approach is known for producing high-quality output voltages with little harmonic distortion. Its mathematical underpinnings and implementation issues are explained. Alternative methods include AZSPWM, which deliberately omits zero voltage vectors to decrease CMV. The NSPWM approach, which manipulates the neutral point voltage, is being investigated for CMV reduction. Performance measures such CMV magnitude, harmonic content, motor efficiency, and switching losses are used to compare. Simulation findings show how each strategy mitigates CMV and affects motor function. Simulation results support simulation findings and reveal real-world applicability and practical obstacles. This paper helps explain the pros and cons of SVPWM, AZSPWM, and NSPWM for CMV reduction. This research suggests using these insights to choose an effective PWM approach for induction motor drives depending on application needs. This study advances motor drive technology for efficient, dependable, and low-interference industrial and commercial applications.

KEYWORDS: Common mode voltage (CMV), SVPWM, AZSPWM and NSPWM

1. INTRODUCTION:

By boosting the switching frequency of the inverter control, rapid switching semiconductor devices like IGBT increase the dynamic performance of pwm inverter fed ac motor drives. A number of unforeseen problems have also been raised as a result of this rapid advancement, including transmitted EMI, shaft voltages, bearing currents, and motor insulation failure [1-2].The underlying source of the aforementioned problems is the internal CMV generation of the inverter. The CMV has decreased as a result of several advances in research. In the conventional vector control method, the instantaneous stator current error signals and hysteresis controllers are employed to produce the gating pulses. Hysteresis current controllers enable the inverter to function with a range of switching frequencies when using the conventional vector control method [3]. These PWM techniques are used to regulate the output voltage

as well as the switching of the inverter. Since every method has advantages and disadvantages of its own, the optimum strategy should be selected for a certain application. It offers improved performance compared to other PWM techniques such as SVPWM and AZSPWM. Additionally, NSPWM is particularly effective in reducing common mode voltage induction in motor driving applications, making it a preferred choice in such scenarios[4-5]. The detailed discussion of these algorithms can be found in [6-7], where their advantages and applications are thoroughly explored. This strategy also results in high level CMV fluctuations because zero voltage vectors exist [8–9]. The complexity of the traditional SVPWM method has been reduced by using a novel SVPWM technique that makes use of hypothetical switching timings, although it still exhibits considerable CMV variations. Recent research has focused on using a PWM method to lower the CMV [11–12].Although these techniques reduce CMV, they complicate the PWM algorithm since they compute switching times using a conventional approach. Open loop v/f control was also employed in these methods. In order to reduce the CMV and complexity associated with PWM algorithms, this study offers a simpler near state PWM algorithm (NSPWM) and active zero state based PWM algorithm (AZPWM). Instead of using the near state PWM algorithm (NSPWM), the suggested PWM algorithms boost the efficiency of induction motors by reducing CMV, decreasing THD values, and enhancing power quality [10]. When compared to other PWM systems, Near State PWM (NSPWM) offers a more user-friendly implementation and has the capacity to considerably lower common mode voltage (CMV) in induction motor drives. NSPWM does this by including a neutral state within the PWM modulation waveform. By reducing the voltage imbalance between the motor phases, this decreases the CMV. NSPWM reduces CMV by actively managing motor phase voltage states.[14] NSPWM smoothes and balances voltage transitions between phases by adding a near state to the PWM pattern, reducing voltage spikes and CMV production [15].

- NSPWM streamlines modulation by adding a close state to the usual active voltage states. Compared to techniques like SVPWM and AZSPWM, NSPWM has a simpler PWM generation algorithm and lower computational requirements, making it ideal for real-time implementation in microcontrollers or digital signal processors in motor drive systems. This can improve hardware design efficiency and cost.
- NSPWM's balanced voltage transitions reduce switching losses in power electronics, enhancing motor drive system efficiency.
- NSPWM reduces CMV, reducing EMI emissions and improving motor drive system EMC properties. This is crucial in EMI-compliant applications.
- NSPWM balances CMV reduction efficacy with implementation complexity, providing a viable method without excessive computational or hardware demands.
- NSPWM's simplicity and efficacy make it suitable for various induction motor drive systems, such as variable frequency drives in industrial, commercial, and residential contexts.

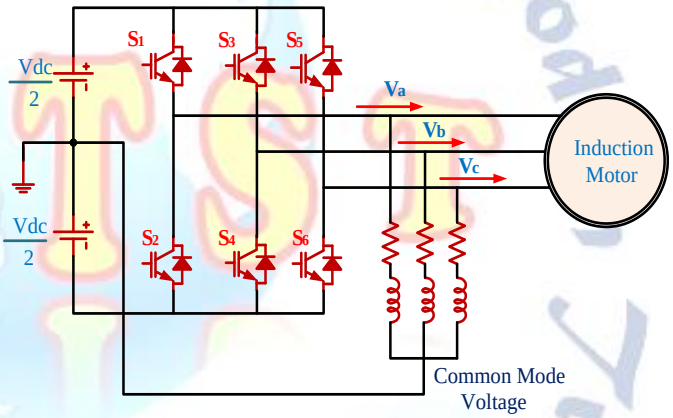


Fig. 1.Common mode Three phase voltage source inverter

2. CONFIGURATION OF PROPOSED SYSTEM

A power electronics inverter is used to convert a DC voltage source (usually a DC bus) into a three-phase AC output to drive the induction motor. The inverter comprises power semiconductor devices (such as IGBTs or MOSFETs) that are controlled using the selected PWM technique. The heart of the system is the three-phase induction motor, which serves as the load. It is a key component that responds to the PWM signals and generates the desired mechanical output. The inverter implements the SVPWM algorithm to generate the necessary voltage vectors for the inverter. The algorithm calculates the duty cycles of the upper and lower switches of each phase to achieve the desired output voltage. The AZSPWM technique involves modulating the inverter switches based on the active zero state

approach. The inverter generates the appropriate control signals to achieve CMV reduction through this method. The NSPWM technique introduces a near state in the PWM pattern to balance the voltage transitions. The inverter generates the switching patterns that incorporate this near state. The entire system is modeled and simulated using appropriate software tools (such as MATLAB/Simulink). Simulation allows for accurate assessment and comparison of CMV reduction and motor performance under different operating conditions.

3. COMMON MODE VOLTAGE (CMV)

The most common two-level voltage source inverter (VSI) includes three switching variables, a, b, and c, one for each inverter phase. For the three steps considered together, there are eight potential switching state combinations. A VSI may produce two zero voltage vectors and six non-zero voltage vectors, as shown in Fig. 1.

Space vectors may be used to express the nth voltage vector as

$$V_n = \frac{2}{3} V_{dc} \exp\left[j(n-1)\frac{\pi}{3}\right]; n = 1,2,3 \ldots 6 \qquad (1)$$

The common mode voltage of a typical three-phase, two-level voltage source inverter may be written as

$$V_{n0} = \frac{V_{a0}+V_{b0}+V_{c0}}{3} \qquad (2)$$

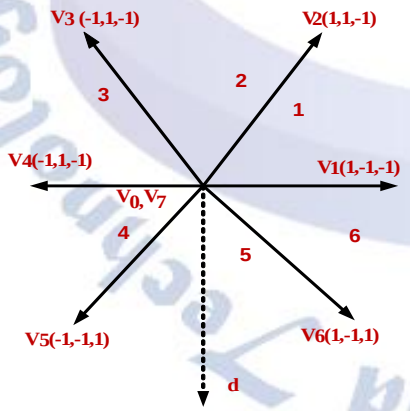


Fig 2 Voltage vectors of VSI

where Va0, Vb0, and Vc0 are the voltages on the inverter's poles. The instantaneous values of CMV may be computed using the switching states described in [12] when the drive is provided by an inverter using the PWM technique and CMV is not zero.

4. PROPOSED PWM ALGORITHMS

The essential premise of SVPWM is that a sinusoidal stimulus will cause the voltage space vector to spin at a constant speed with a circle at its point. The eight switching configurations are denoted by the letters V0(000),V1(100),V2(110),V3(010),V4(011),V5(001),V6(101), and V7(111) and are made up of the six switches that make up a two-level inverter. If the three binary digits have a value of 1, the top transistor is closed; if they have a value of 0, the bottom transistor is closed. The three binary digits each correspond to a single bridge leg. In Fig. 4, the six active voltage vectors (V_1 –V_6) out of the eight vectors are shown as being situated along a hexagon's axis, whereas V0 and V7 are two zero states. Any pair of subsequent non-zero vectors has an angle of 60 degrees with one another. As shown in fig. 3, SVPWM requires the instantaneous amplitude of Vref and angle in order to calculate switching intervals T_1, T_2, and T_0.

A. Implementation of SVPWM

The voltage equations in the ABC reference frame are converted into the stationary d-q reference frame, which is made up of the horizontal (d) and vertical (q) axes, in order to execute space vector PWM. The reference voltage vector is created from the two-phase vectors and translated into two reference frames using the Parks transform. The Volt-second balancing idea is a method for implementing space vector PWM. Equation 3 is used to get the angle after transforming the voltagesV_a, V_b, V_c into the d-q reference frame as V_d , V_q using the appropriate transformation formulae.

$$\alpha = \tan^{-1}\left(\frac{V_q}{V_d}\right) \qquad (3)$$

According to the volt-second balancing idea, if the reference voltage vector is in sector 1 (0° to 60°), switching between the vectors in the states 100, 110, and zero will take place, as shown in Fig. 3. After applying vectors V_1 and V_2 , which each produce periods of T_1 and T_2 seconds, zero vectors are utilised for the remaining time (T_0) seconds. V_0 and V_7 are zero-vector applications with identical time. The changeover time may be calculated using equations 5 through 7.

$$T_z = T_1 + T_2 + T_3 \qquad (4)$$

Where Tz is the total time period.

$$T_1 = T_z \times A \times \frac{\sin\left(\frac{\pi}{3} - \alpha\right)}{\sin\left(\frac{\pi}{3}\right)} \quad (5)$$

$$T_1 = T_z \times A \times \frac{\sin(\alpha)}{\sin\left(\frac{\pi}{3}\right)} \quad (6)$$

$$T_0 = T_z - (T_1 + T_2) \quad (7)$$

$$A = \frac{V_{ref}}{V_{dc}} \quad (8)$$

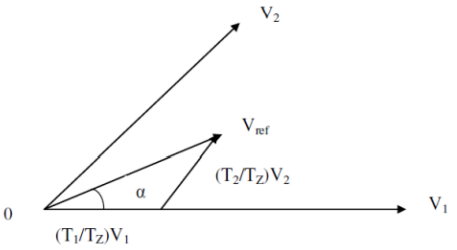


Fig 3: Combining neighboring vectors at sector 1, the reference vector is at that location.

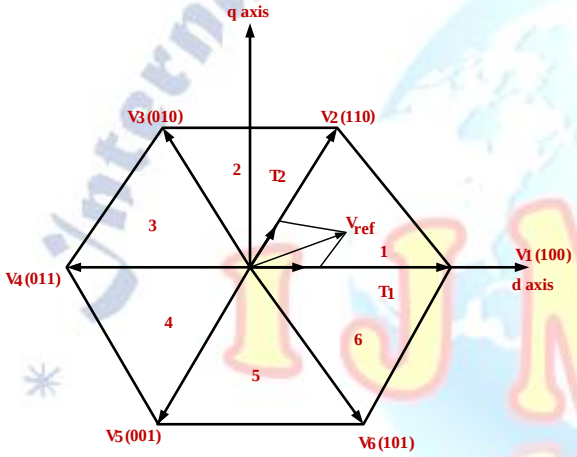


Fig 4: distinct sections of space voltage vectors

B. Implementation of AZSPWM

Comparing the recommended AZS to the conventional VSI, the difficulty of hardware modification is not noticeably increased. More importantly, the suggested AZS inherits the benefit of zero CMV when activated as opposed to interfering with the usage of any existing PWM strategy. SVPWM's superior qualities have led to it being the norm for motor driving. A minor change to the modulation approach is needed to reduce CMV with the proposed AZS: As seen in Fig. 5, the hexagonal area covered by all nine potential space vectors remains intact. It is recommended to avoid synthesizing output voltage Vref using voltage vectors V_0 and V_7; instead, voltage vector V_8 should be used in their place. Similarly, for Vref, who resides in sector VI, the following equations (5) and (6) apply:

$$V_{ref}\,T_s = V_5 T_5 + V_4 T_4 + V_8 T_8 \quad (9)$$

$$T_s = T_5 + T_4 + T_8 \quad (10)$$

Where T8 is the d well time for new voltage vector V8 when the proposed AZS is in use. The resultant CMV waveform in one sampling period is shown in Fig. 5. However summarized the inverter output and CMV at each state for conventional three-phase VSI equipped with proposed AZS.

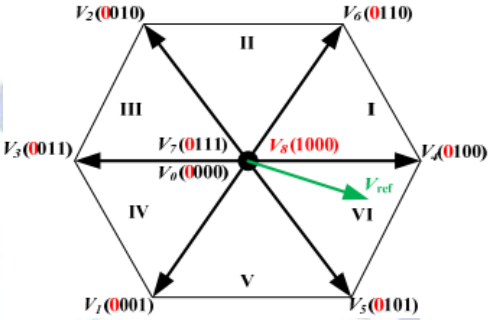


Fig.5. Nine space voltage vectors in the complex plane for a VSI with AZS.

C. Implementation of NSPWM

A series of three neighboring voltage vectors are used in the Near State PWM (NSPWM) approach to match the output and reference volt-seconds. These three voltage vectors are selected in order to employ the voltage vector that is closest to the reference voltage vector as well as its two neighbors (to the right and left). As a consequence, the voltage vectors in the space change every 60 degrees. T_0 Implement the strategy, the voltage vector space is divided into six parts, as illustrated in Fig. 6. For area Bi, voltage vectors V_{i}-1, V_{i}, and V_{i}+1 determined by indices are employed. For the region (B2) between 30^0 and 90^0 (Fig. 7), the applied voltage vectors, for example, are V_1, V_2, and V_3.

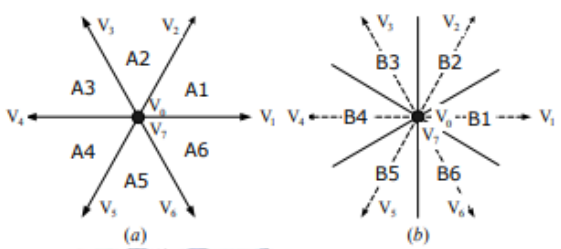


Fig. 6. Voltage space vectors and 60o sector definitions.

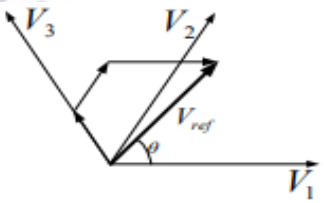


Fig.7. Illustration of the NSPWM space vectors for B2.

The reference voltage vector is produced utilizing the near state PWM (NSPWM) approach by combining three

neighbor voltage vectors. The suggested NSPWM algorithm does not use zero voltage vectors in order to lessen common mode voltage discrepancies. As the voltage vectors closest to the reference voltage vector and its two neighbors in each sector, these three voltage vectors were selected. Thus, the voltage vectors in use are modified by each sector. The voltage vector space is partitioned into six sectors as shown in Fig. 8 in order to perform the procedure. The subject in this case likewise only applies to the first sector since all six sectors are symmetric. Given the necessary reference voltage vector, the formulas in (11) (12) and (13) may be utilized to determine the timings of the active voltage vectors (V_1, V_2, and V_6).

$$T_1 = \left\{-1 + \frac{3}{\pi} M_{\bar{i}} \cos\left(\alpha + \frac{\pi}{3}\right) + \frac{3\sqrt{3}}{\pi} M_{\bar{i}} \sin\left(\alpha + \frac{\pi}{3}\right)\right\} T_s \quad (11)$$

$$T_2 = \left\{1 - \frac{3}{\pi} M_{\bar{i}} \cos\left(\alpha + \frac{\pi}{3}\right) - \frac{\sqrt{3}}{\pi} M_{\bar{i}} \sin\left(\alpha + \frac{\pi}{3}\right)\right\} T_s \quad (12)$$

$$T_6 = T_s - T_1 - T_2 \quad (13)$$

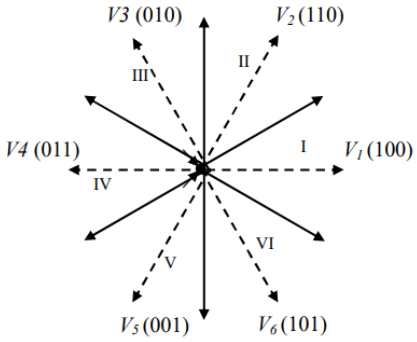
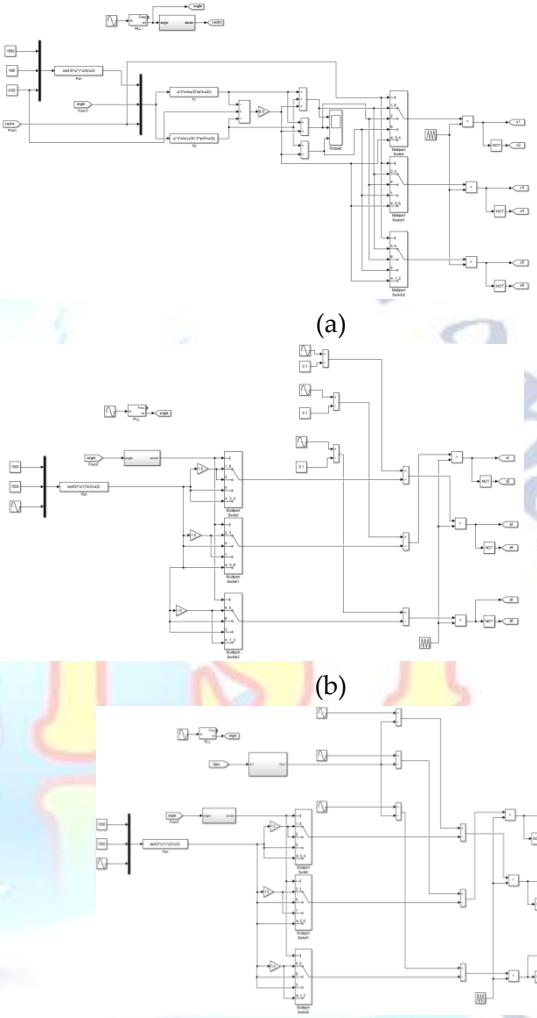


Fig. 8 Possible voltage space vectors and sector definition in NSPWM algorithm

However, the NSPWM method's answers to equations (11), (12), and (13) are accurate when the modulation index fluctuates between 0.61 and 0.906 [10]. To obtain the lowest switching frequency and lowest common mode voltage, the NSPWM algorithm uses 216-612 in sector-I, 321-123 in sector-II, and so on. The SVPWM algorithm creates a total of three commutations throughout a sampling time period, while the NSPWM technique only generates two. Additionally, any one of the phases is clamped to either the positive or negative DC bus for a maximum of 1200 times per a fundamental cycle since the modulating waveform of the NSPWM algorithm matches the DPWM1 waveform. As a consequence, switching losses on the associated inverter leg are decreased. As a consequence, the switching frequency of the NSPWM algorithms is 33% lower than that of the SVPWM algorithms.

5. INDUCTION MOTOR DRIVE WITH GSPWM ALGORITHM BASED VECTOR CONTROL



(a)

(b)

(c)

Fig. 9 control simulation design of (a) SVPWM, (b) AZSPWM, (c) NSPWM

6. SIMULATION RESULTS

A. Performance of the induction motor drive system in a steady state

A numerical simulation using Matlab/Simulink has been done to validate the suggested strategy. This case study's induction motor is a three-phase squirrel cage induction motor. The simulation includes various operating conditions such as different load torque values and varying input voltages. Additionally, the simulation takes into account the motor's electrical and mechanical parameters to accurately represent its behavior in real-world scenarios.

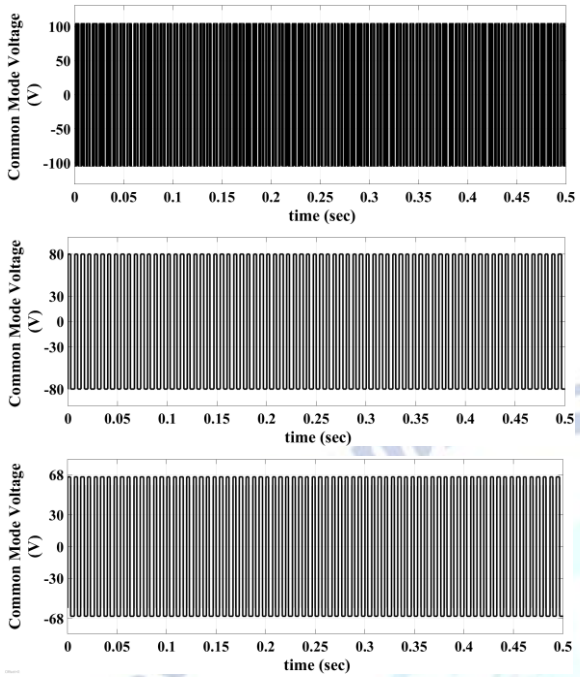


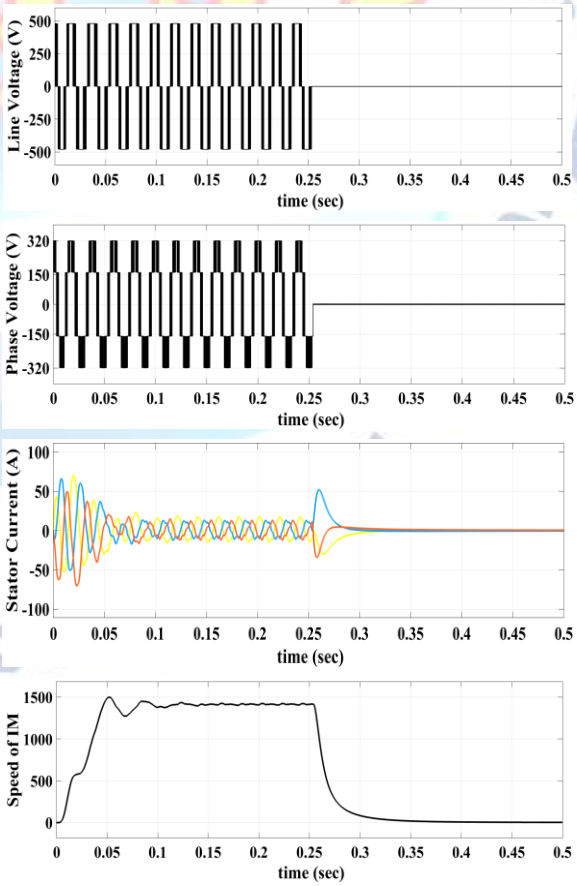
Fig.10 common mode voltage comparison between SVPWM, AZSPWM, and NSPWM

On the subject of lowering common mode voltage and enhancing system stability, power quality, and total harmonic distortion, these solutions have been thoroughly examined and compared. The findings revealed that the AZSPWM method was able to reduce common mode voltage by 80 volts while the SVPWM method was able to reduce it by 106 volts. The highest result, as well as a notable reduction of 66 volts in common mode voltage, was achieved using the NSPWM approach. According to these results, the common mode voltage may be decreased using SVPWM, AZSPWM, and NSPWM approaches. Apart from that, the findings imply that NSPWM may be the method that offers the best chances of attaining considerable reductions in common mode voltage. All three strategies saw a considerable drop in the common mode voltage relative to the starting point. The efficacy of SVPWM, AZSPWM, and NSPWM in lowering common mode voltage, with NSPWM demonstrating the largest decrease among them, is clearly seen in Figure 10.

B. Dynamic Performance of GSPWM Induction Motor Drive System

This paper presents a comprehensive comparative analysis of three prominent PWM techniques: Space Vector Pulse Width Modulation (SVPWM), Active Zero State PWM (AZSPWM), and Near State PWM (NSPWM), with the objective of reduction CMV in induction motor drives. The study encompasses both theoretical investigation and practical validation using simulation. The SVPWM technique is renowned for its ability to produce high-quality output voltages with reduced harmonic distortion. It is discussed in terms of its mathematical foundation and implementation challenges. The AZSPWM technique, which selectively omits certain zero voltage vectors in order to reduce CMV, is presented as an alternative approach. Furthermore, the NSPWM technique, based on the manipulation of the neutral point voltage, is explored for its potential in CMV reduction. The comparative analysis is carried out based on several performance metrics, including CMV magnitude, harmonic content, motor efficiency, and switching losses. Simulation results demonstrate the effectiveness of each technique in mitigating CMV and their impact on motor performance. Simulation results corroborate the simulation findings and provide insights into real-world applicability and practical challenges.

a. Dynamic performance of SVPWM



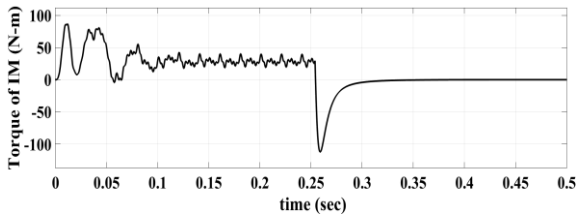


Fig.11 dynamic performance of SVPWM technique for common mode voltage induction motor drive

b. Dynamic performance of AZSPWM

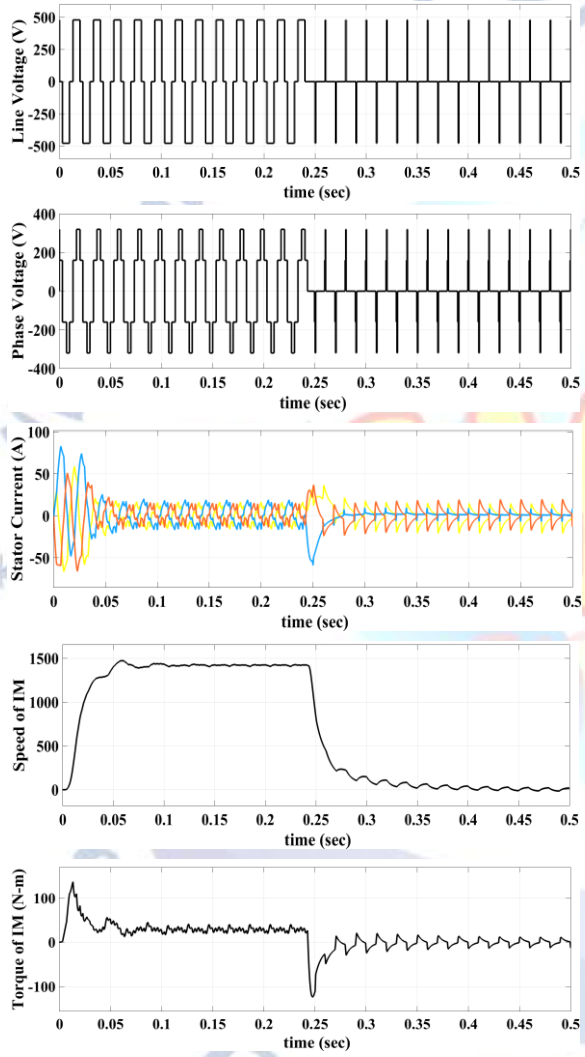
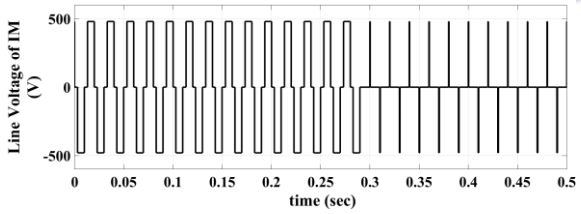


Fig.12 dynamic performance of AZSPWM technique for common mode voltage induction motor drive

c. Dynamic performance of NSPWM



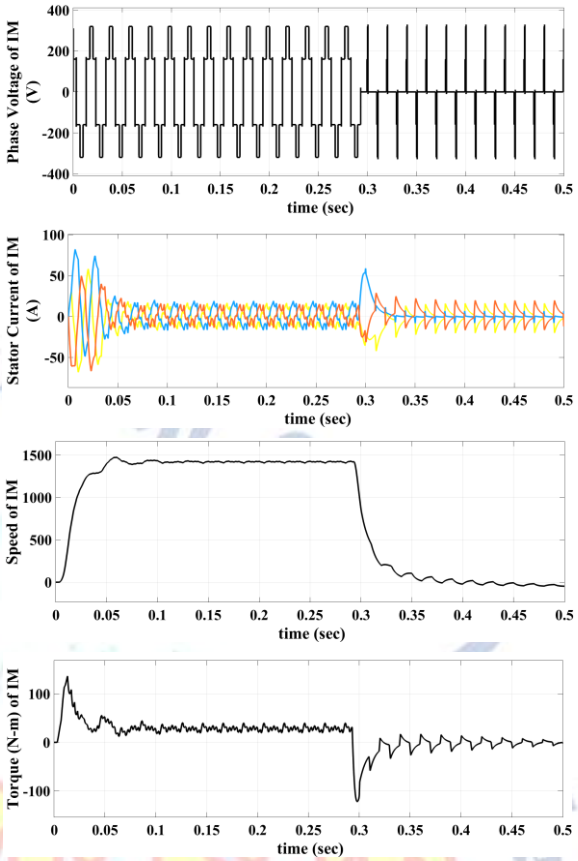


Fig.13 dynamic performance of NSPWM technique for common mode voltage induction motor drive

However, by implementing pulse width modulation (PWM) techniques, the control of the induction motor's dynamic performance can be enhanced. PWM allows for precise adjustment of the motor's speed, torque, and phase voltage, line voltage and stator current resulting in improved control and stability. Additionally, Figure (11-13) illustrates how these parameters may vary when PWM is utilized.

7. CONCLUSION

Performance and usefulness of SVPWM, AZSPWM, and NSPWM for common mode voltage reduction in induction motor drives are discussed. Each modulation technique has benefits and drawbacks, thus the selection should be based on the application and system constraints. SVPWM is a tried-and-true technique for efficiently using voltage. It is suitable for applications demanding strong torque and low harmonics because to its balanced and low harmonic output voltages. Certain applications could be hampered by the technical complexity and need for precise control techniques. High-performance drive systems requiring precise

control benefit greatly from SVPWM. AZSPWM is a quick and efficient approach to lower common mode voltage. By eliminating the zero-sequence voltage component, electromagnetic interference is reduced to a minimum. For applications requiring modest performance, AZSPWM is easy to implement and reasonably priced. It might consume less voltage and have more output harmonic distortion than SVPWM. Using induction motor commutation, NSPWM lowers common mode voltage. It is perfect for simple applications and requires less complicated control. NSPWM could have constraints on torque ripple reduction and harmonic performance in comparison to SVPWM. It performs effectively in applications with modest performance that make advantage of the induction motor's inherent characteristics. In conclusion, the requirements of the induction motor drive system dictate whether to use SVPWM, AZSPWM, or NSPWM. For high-performance applications needing precise control and low harmonics, SVPWM is dependable. For less demanding applications, AZSPWM decreases common mode voltage more easily and affordably. NSPWM balances complexity and performance by reducing common mode voltage utilising motor attributes. For each induction motor driving application, system designers and engineers must consider cost, performance, and complexity to choose the appropriate modulation approach.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

REFERENCES

[1] Y.Murai, T.Kubota, and Y.Kawase, "Leakage current reduction for a high-frequency carrier inverter feeding an induction motor," IEEE Trans. Ind. Appl., vol. 28, no.4, Jul./Aug. 1992, pp. 858-863.

[2] .J.Erdman, R.J.Kerkman, D.W.Schlegel, and G. L. Skibinski, "Effect ofPWM inverters on AC motor bearing currents and shaft voltages",IEEE Trans. Ind. Applicat., VOL. 32,Mar/Apr. 1996, pp,250-259.

[3] Yen-Shin Lai, "Investigations into the effects of PWM techniques on common mode voltage for inverter-controlled induction motor drives", Power Engineering Society 1999 Winter Meeting, IEEE, col. 1, 1999, pp.35-40.

[4] M.M.Swamy, K.Yamada, and T.Kume, "Common mode current attenuation techniques for use with PWM drives," IEEE Trans. Power Electron., vol. 16, no.2, Mar. 2001, pp. 248-255.

[5] S.Ogasawara, H.Ayano, and H.Akagi, "An active circuit for cancellation of common –mode voltage generated by a PWM inverter," IEEE Trans.Power Electron., vol. 13, no.5, Sep. 1998, pp. 835-841.

[6] Domenico Casadei, Francesco Profumo, Giovanni Serra, and Angelo.Tani, "FOC and DTC: Two Viable Schemes for Induction Motors Torque Control" IEEE Trans. Power Electron., vol. 17, no.5, Sep, 2002, pp. 779-787

[7] Isao Takahashi and Toshihiko Noguchi, "A new quick-response and high-efficiency control strategy of an induction motor," IEEE Trans.Ind. Applicat., vol. IA-22, no.5, Sep/Oct 1986, pp. 820-827

[8] Thomas G. Habetler, Francesco Profumo Michele Pastorelli and Leon M. Tolbert , "Direct Torque Control of Induction Machines Using Space Vector Modulation", IEEE Trans. Ind. Appl., Vol. 28, No.5, Sep/Oct, 1992, pp. 1045-1053.

[9] Heinz Willi Van Der Broeck, Hans-Christoph Skudelny, Member, IEEE, and Georg Viktor Stanke " Analysis and Realization of a Pulsewidth Modulator Based on Voltage Space Vectors "IEEE Trans. Ind. Appl.,vol.24, no.1,Jan/Feb, 1998

[10] Joohn-Sheok Kim and Seung-Ki Sul, "A novel voltage modulation technique of the space vector PWM" in Proc. IPEC, Yokohama, Japan,1995, pp. 742-747.

[11] Emre Un, Ahmet M.Hava "A Near State PWM Method With Reduced Switching Frequency And Reduced Common M ode Voltage For Three- Phase Voltage Source Inverters" IEEE-IEMDC 2007 Antalya-Turkey, May 2-5, 2007.

[12] Ahmet M.Hava and Emre Un, "Performance Analysis of Reduced Common-Mode Voltage PWM Methods and Comparison With Standard PWM Methods for Three-Phase Voltage-Source Inverters" IEEE Trans. Power Electron., vol. 24, no.1, Jan, 2009, pp. 241-252.

[13] V. Anantha Lakshmi, T. Bramhananda Reddy, G. Naresh Kumar Reddy, M.Surya Kalavathi and V.C.Veera Reddy "Simple and Novel Space Vector Based Voltage Modulation Methods for Reduced Common Mode Voltage in Induction Motor Drives" ICAECT 2010, Jan07 -10, 2010

[14] Emre Ün and A.M. Hava, "A near state PWM method with reduced switching frequency and reduced common mode voltage for three phase voltage source inverters" IEEE-IEMDC, pp. 235-240, May, 2007.

[15] Kandukuri Swathi and K. Swarna Latha, "Common Mode Voltage Reduction for Three Phase Grid Connected Converters using Multi Level Pulse Width Modulation Techniques" IJARIIT 2017,